3D Nanocarbon Interconnects

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Outline

- Introduction
  - Scaling in Integrated Circuits
  - Interconnects versus Transistors
- CNT as 1D Interconnect Structure
- CNT-Graphene for All-Carbon 3D Interconnects
- Summary

Semiconductor Chronology

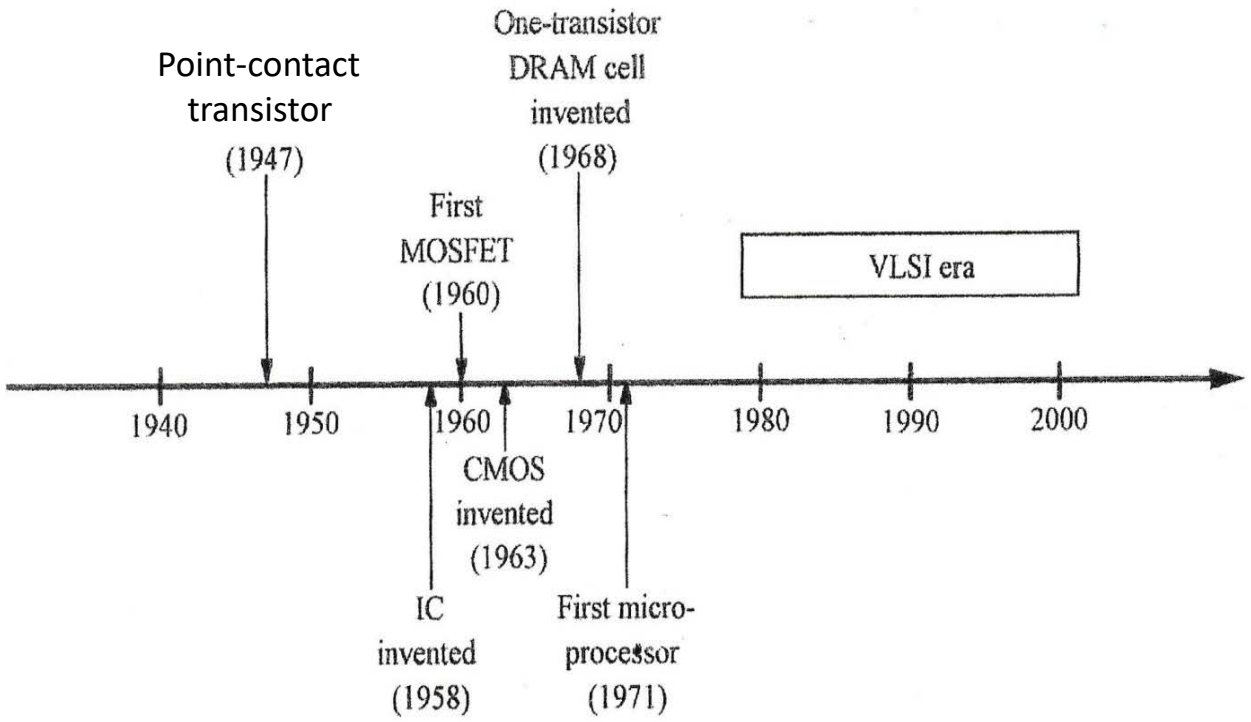


FIGURE 1.1. A brief chronology of the major milestones in the development of VLSI.

Taur & Ning (2009)

Integrated Circuit Trends

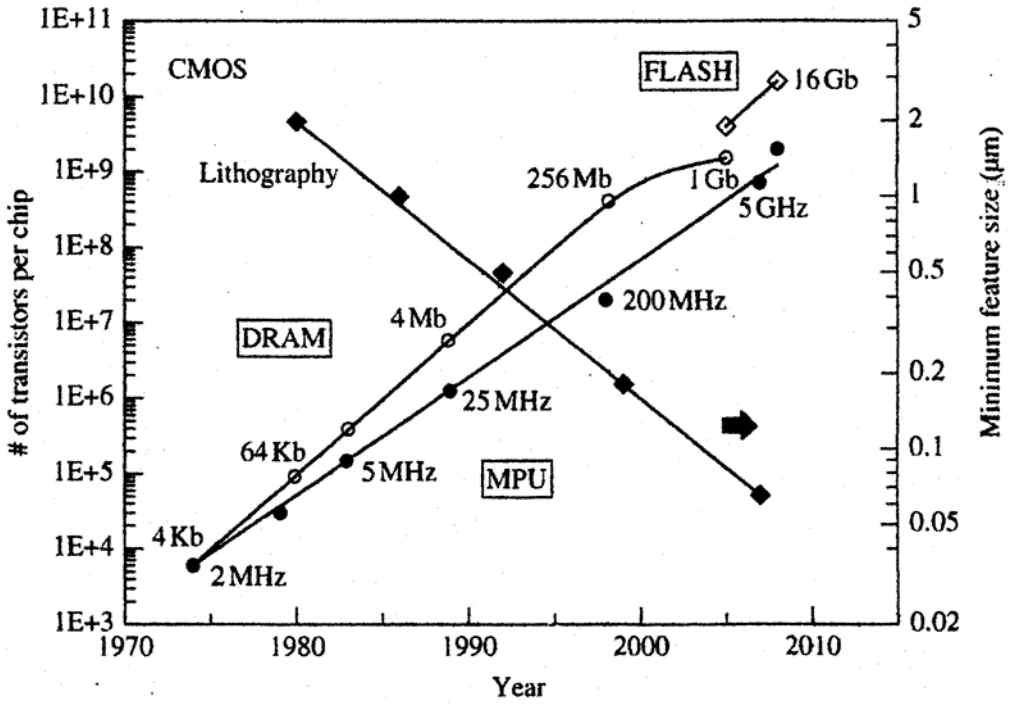
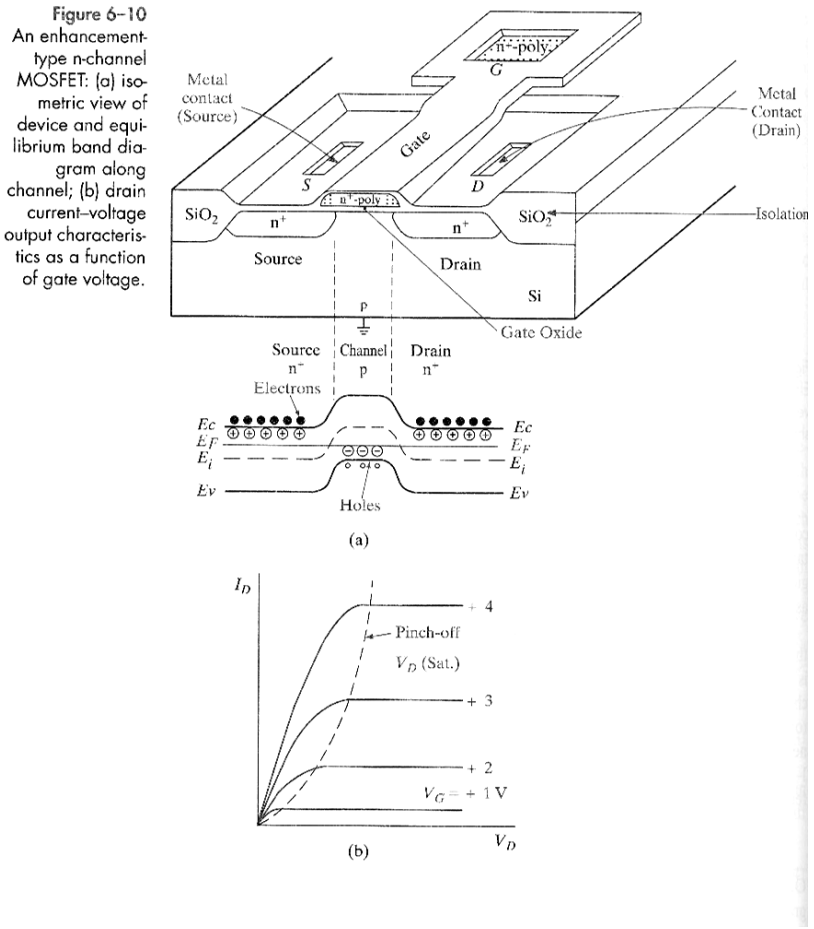
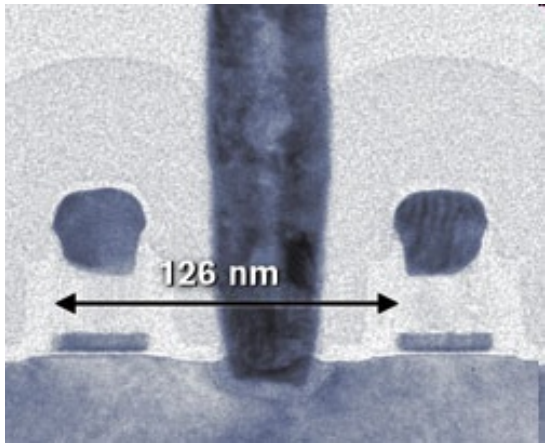


Figure 1.2. Trends in lithographic feature size, number of transistors per chip for DRAM and microprocessors (MPU), and number of memory bits per chip for Flash. The transistor count for DRAM is computed as 1.5 times the number of bits on the chip to account for the peripheral circuits. Recent data points represent announced leading edge products.

Taur & Ning (2009)

MOS Field-Effect Transistor (Planar Technology)



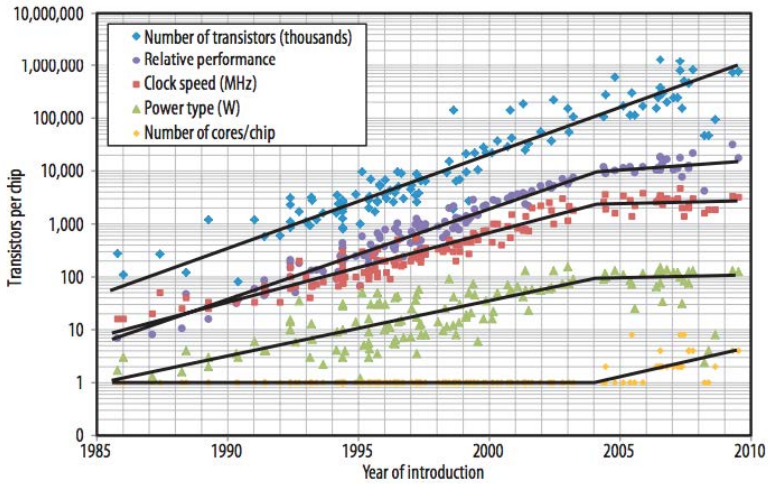


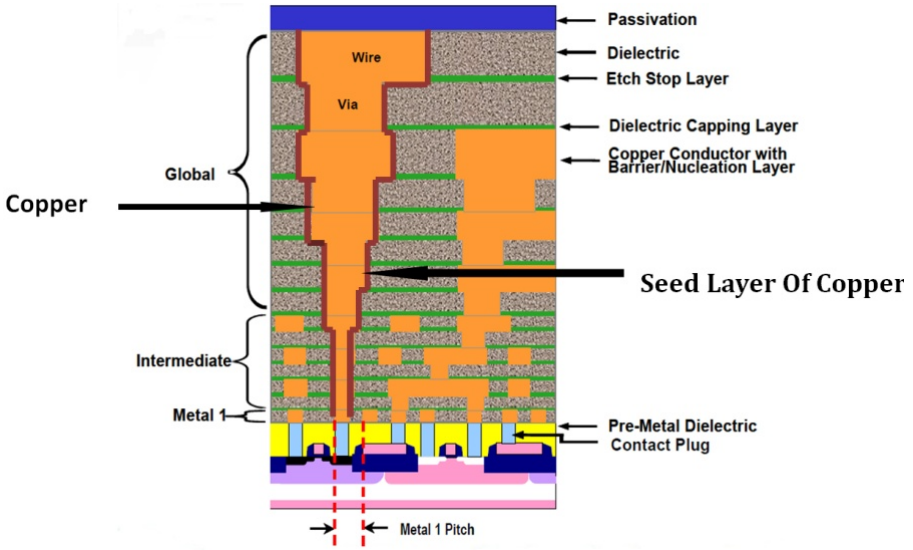
32 nm gate width MOS device shown by IBM at 2007 VLSI meeting. The semiconductor industry believed that the 32 nm litho node will mark the end of the current planar IC technology. Intel moved to **FinFET** in their 22 nm chips in 2011, while TSMC, Samsung, and others did the same subsequently for their 16nm/14nm technologies.

B.G. Streetman and S. Banarjee “Solid State Electronic Devices,” Prentice Hall (2000)

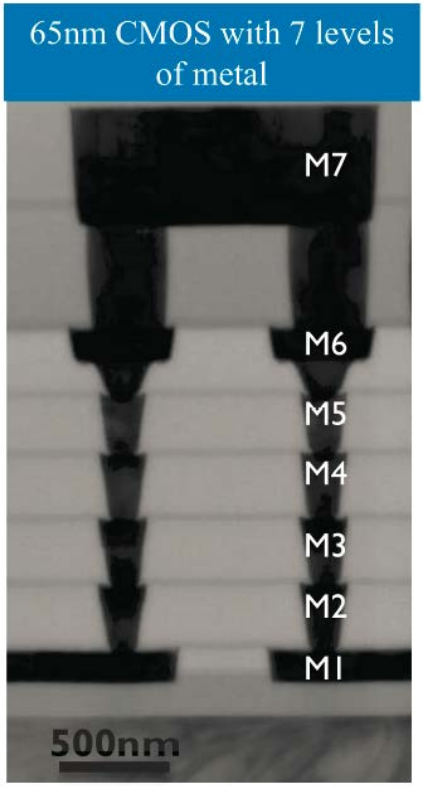
On-chip Scaling driven by Moore's Law

- Doubling number of transistors every two years (Moore 1975)
- Enabling more functions; reducing cost
- On-chip interconnects becoming limiting factor for performance and reliability

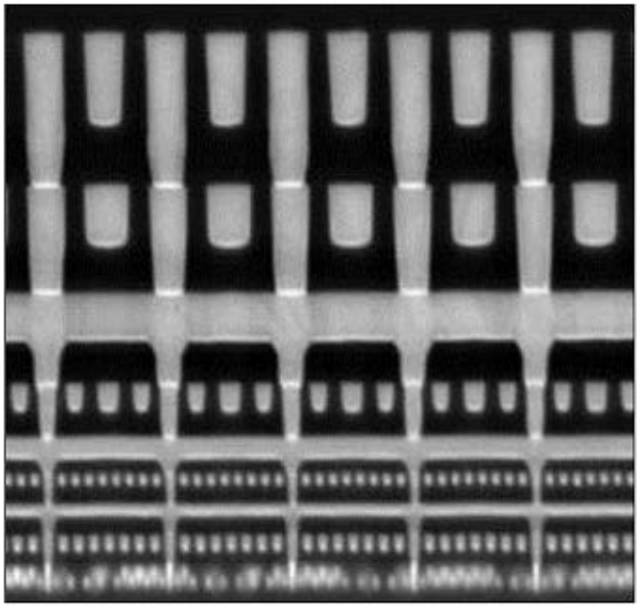




On-chip Interconnects

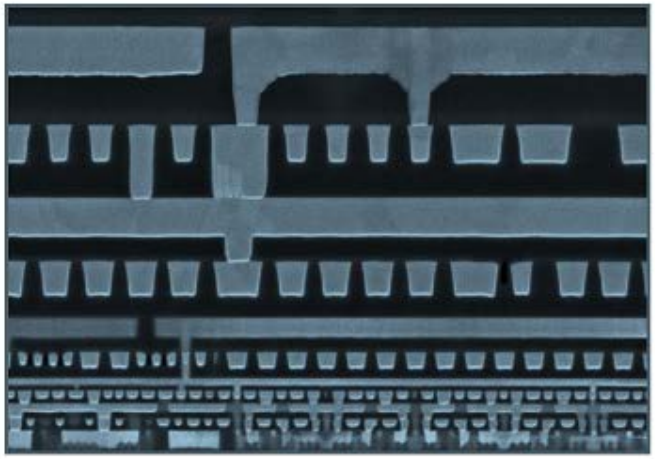


22 nm Process



80 nm minimum pitch

14 nm Process

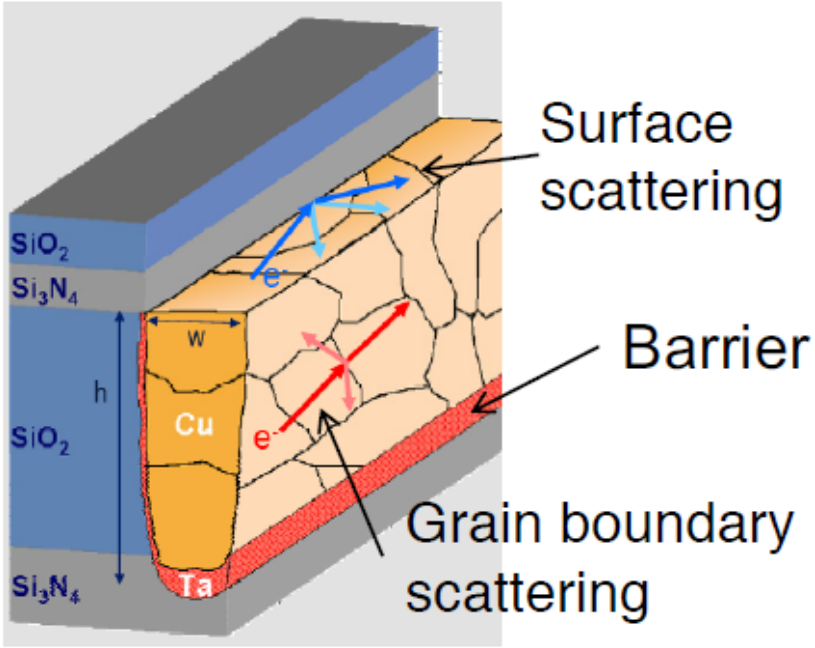


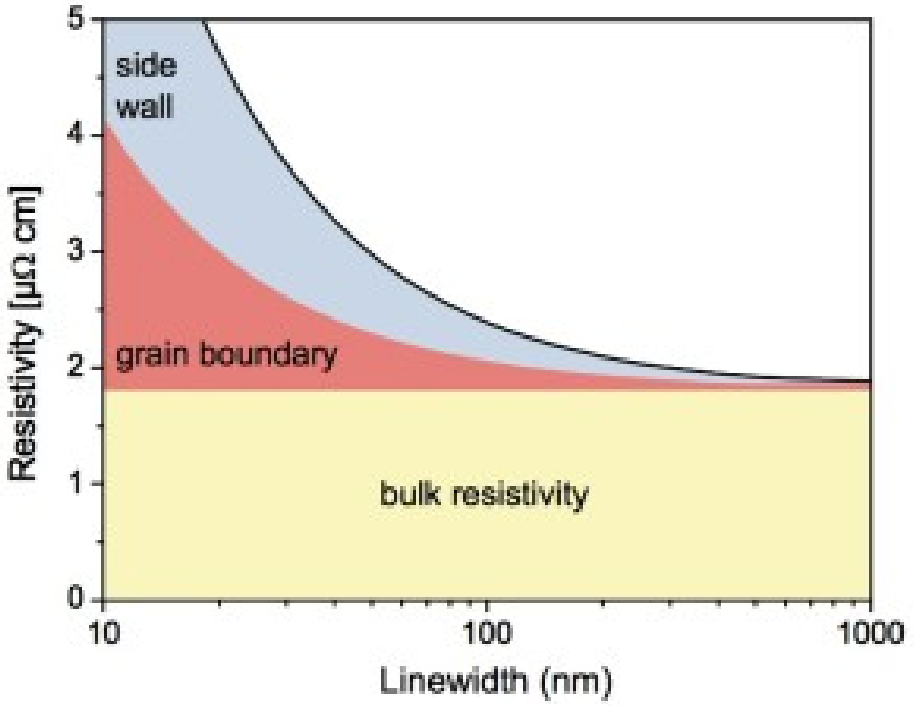
52 nm (0.65x) minimum pitch

Intel 14 nm process press release 9/2014

Effect of Scaling on Interconnect Performance

- **Resistivity of Cu surges with downward scaling**

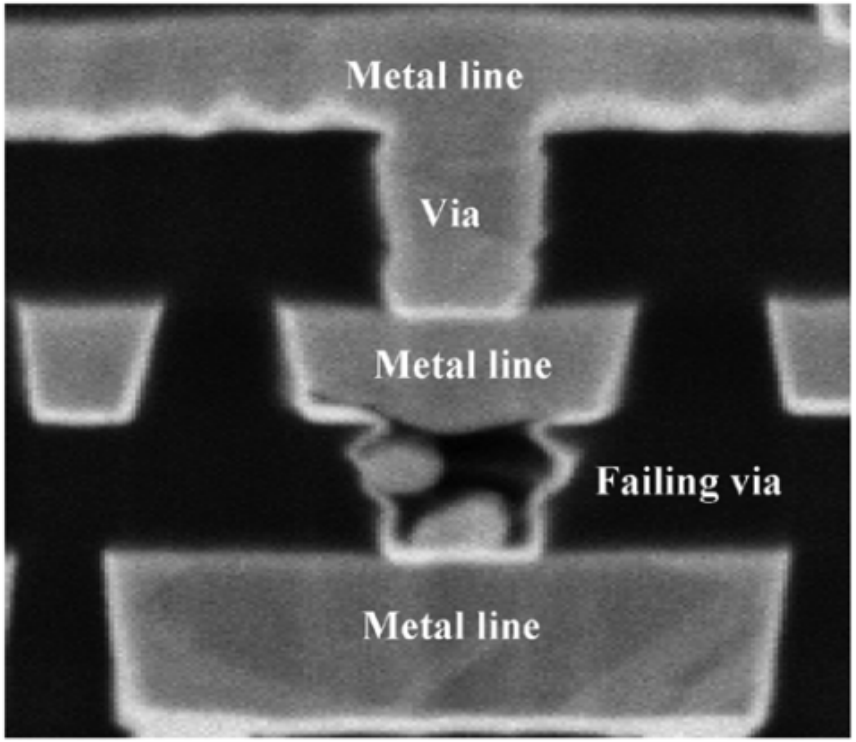




ITRS 2007

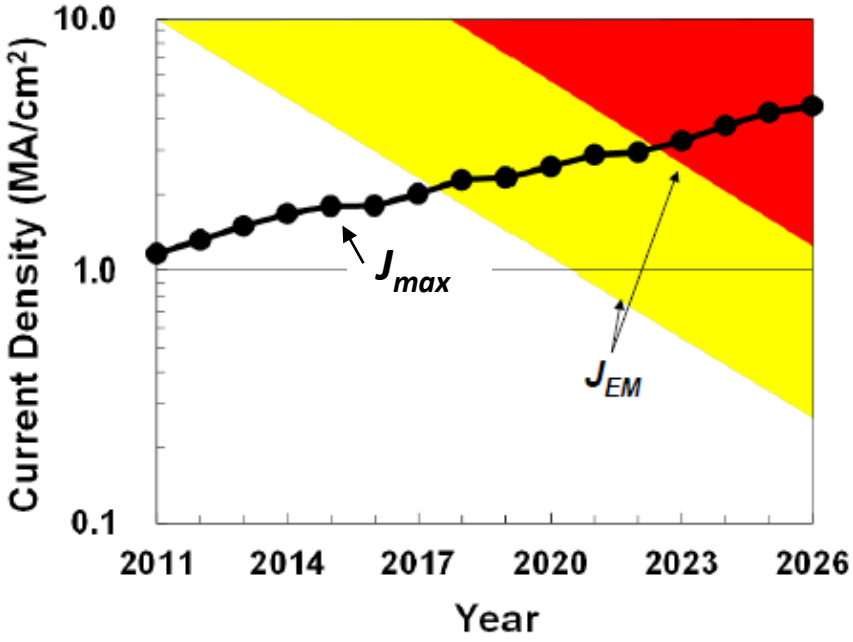
Effect of Scaling on Interconnect Reliability

- **Current density approaching EM limit of Cu interconnects**
- **Voids formed causing failure of interconnects**



SEM image of an electrically failed via

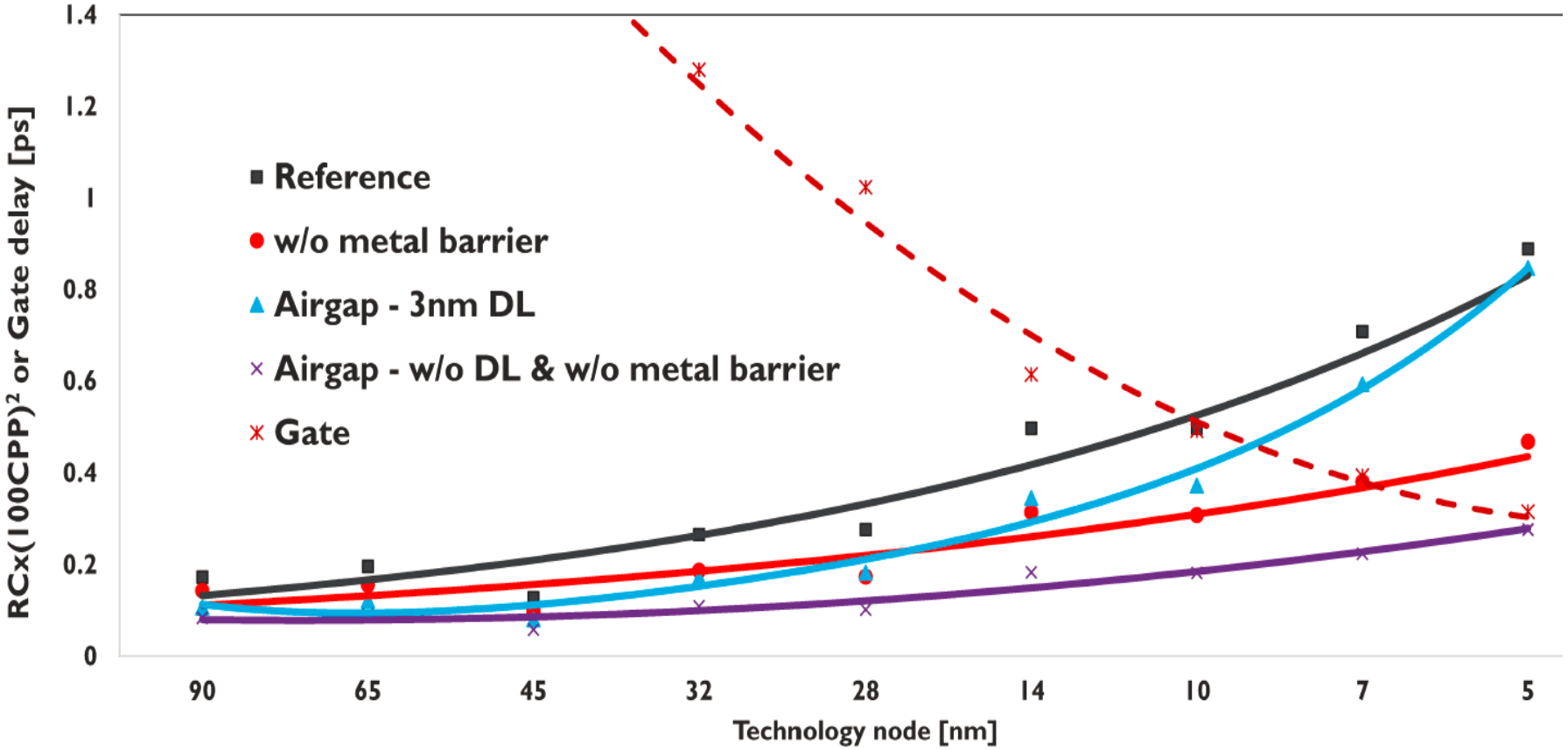
M. A. Hussein, J. He, IEEE Trans. Semicon. Manufacturing 18 (2005)



ITRS 2013

Effect of Scaling on Interconnect Performance

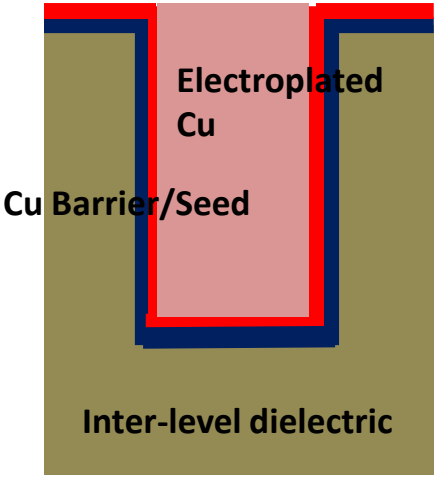
- **RC delay for local interconnects**

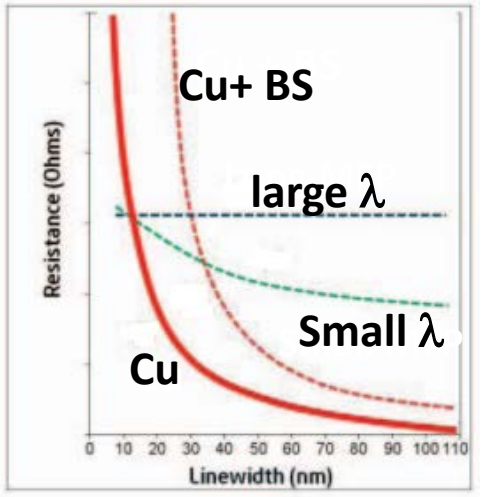


IMEC, IITC 2016

Alternative Interconnect Materials and Structures

- Conductors with electron mean free path λ either significantly larger or smaller than those in Cu and W, and without use of barrier/seed layer
- Current-carrying capacity significantly higher than Cu and W

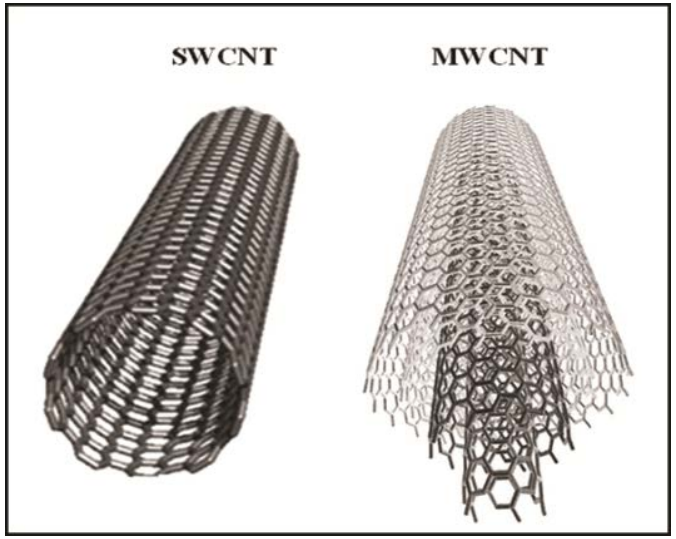


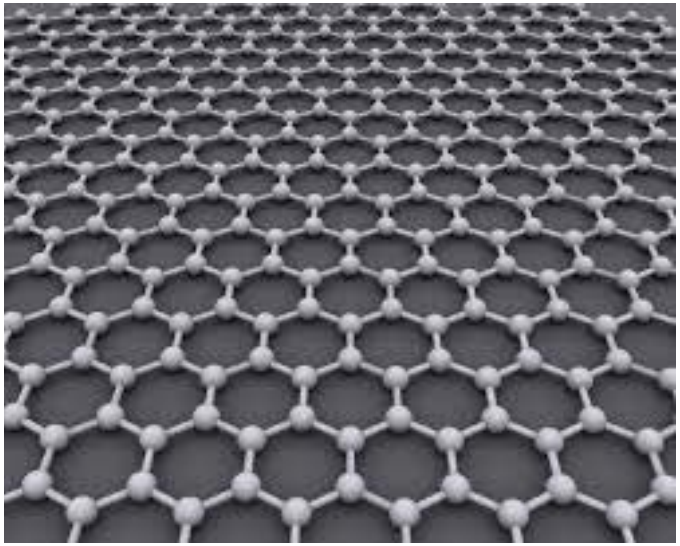


Clarke et al. VLSI 2014

Alternative Interconnect Materials and Structures

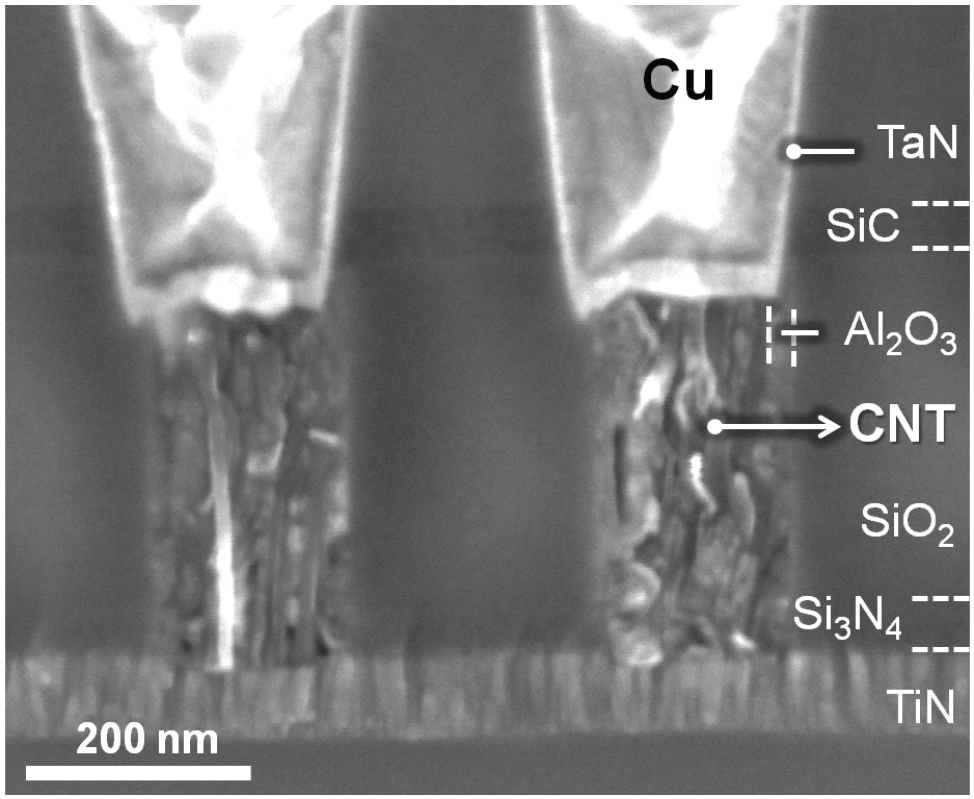
- **Nanocarbons as potential replacements for Cu**
  - **Electromigration-resistant -** Current-carrying capability >10^8 A/cm^2
  - **Long mean free path -** High mobility and near-ballistic transport
  - **High thermal conductivity -** ~ 3000 W/(K·m) (Cu ~ 400 W/(K·m))
  - **Contact resistance challenges**





Alternative Interconnect Materials and Structures

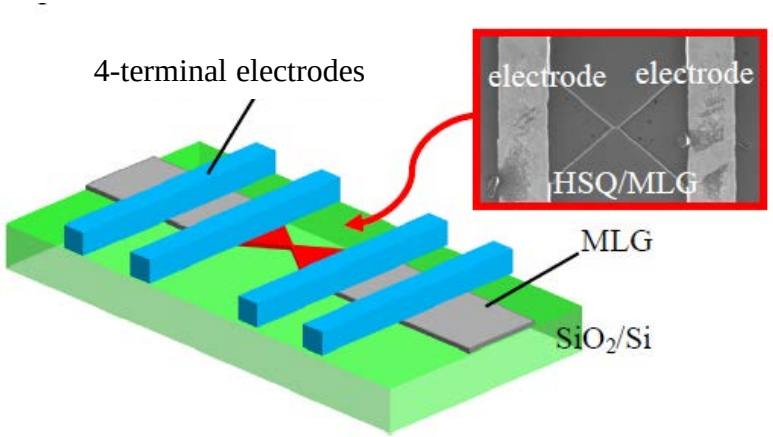
- CNT vias/plugs in local interconnects

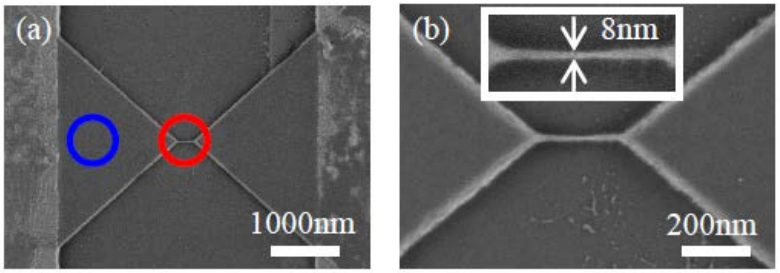


M. H. Van der Veen, et al., *IITC*,189 (2012)

Alternative Interconnect Materials and Structures

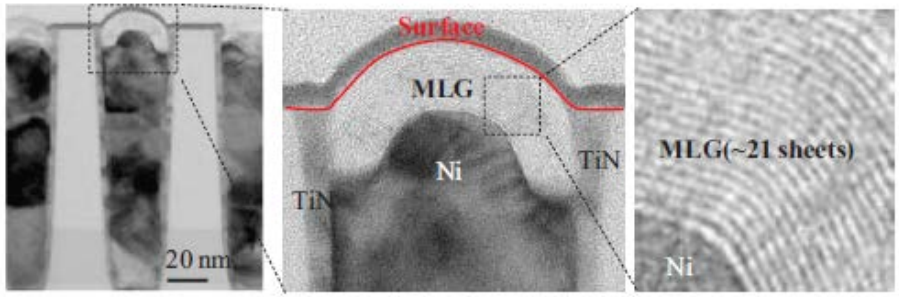
- Graphene interconnects

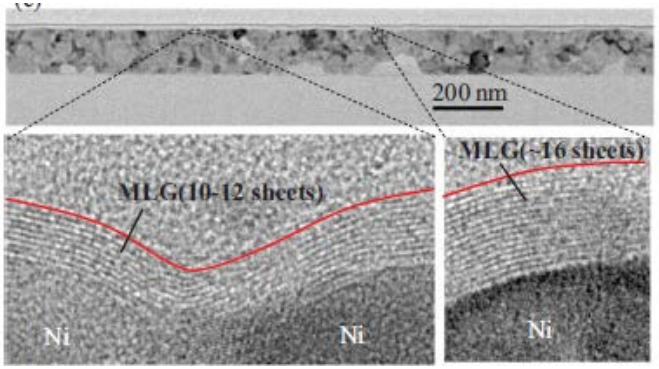




8-nm-wide intercalated MLG: resistivity of 3.2 μΩ cm

D. Kondo, et al., *IITC*,189 (2014)



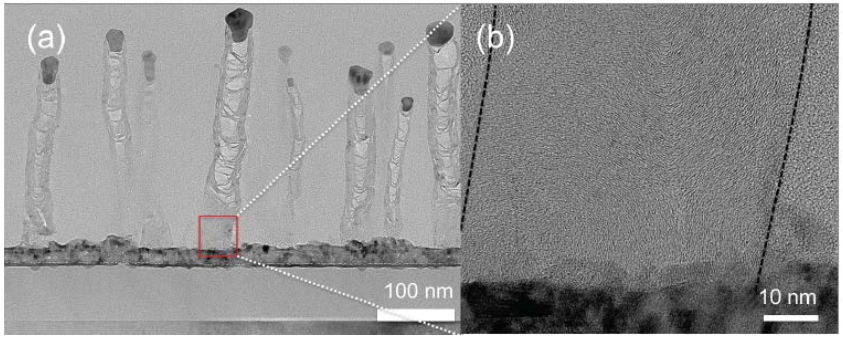


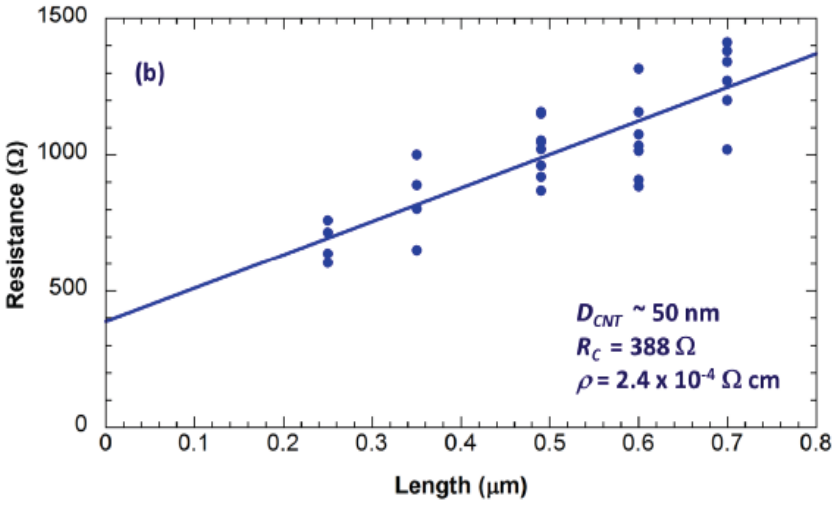
30-nm-width bilayer interconnects of multilayer graphene and Ni

T. Ishikura, et al., *IITC*,321 (2015)

Nanocarbon Interconnects: Contact Resistance Challenges

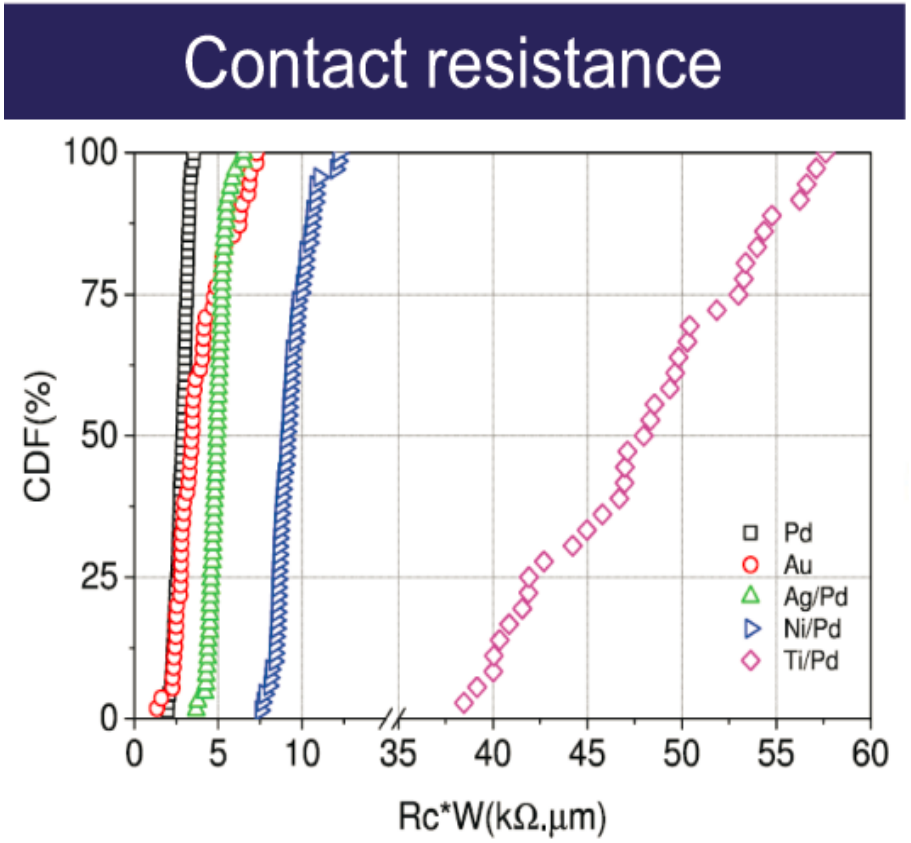
CNT-metal contacts





P. Wilhite, et al., *SST* 29 (2014)

Graphene-metal contacts



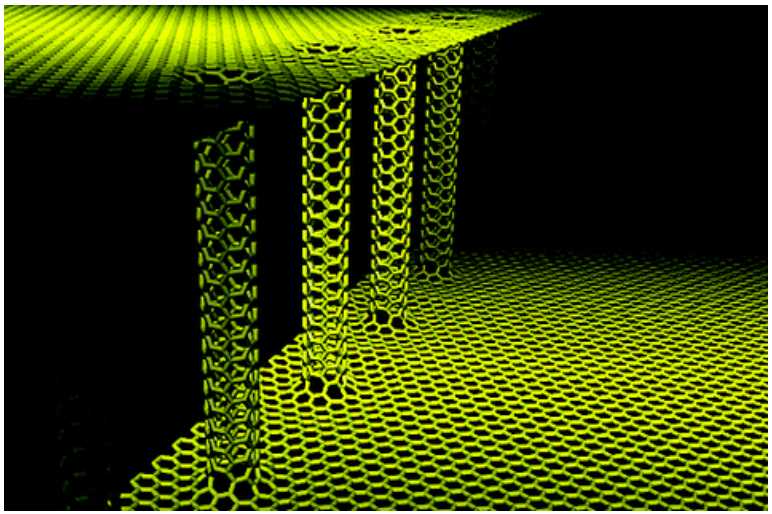
Politou,et al., *APL* 107 (2015)

All-Carbon Interconnects: 1D to 3D

CNT as local vertical interconnect

Graphene as horizontal interconnect and/or active channel material

sp^2-bonded carbon interconnect



Novaes F., et al., *ACS Nano* 4 (2010)

- **Extension of superior nanocarbon properties to 3D integration**
- **sp^2 bonding for high electrical and thermal conductance**

Two Possible Scenarios for Nanocarbon Interconnects

A. Replace completely or partly Cu and W (or Co or Ru) in Si-based chips

B. Integrate into an all-carbon chip

Outline

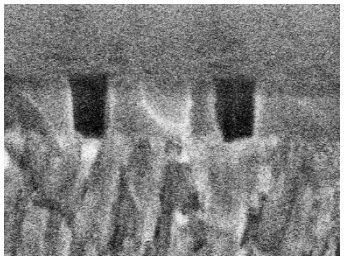
- Introduction
  - Scaling in Integrated Circuits
  - Interconnects versus Transistors
- **CNT as 1D Interconnect Structure**
- CNT-Graphene for All-Carbon 3D Interconnects
- Summary

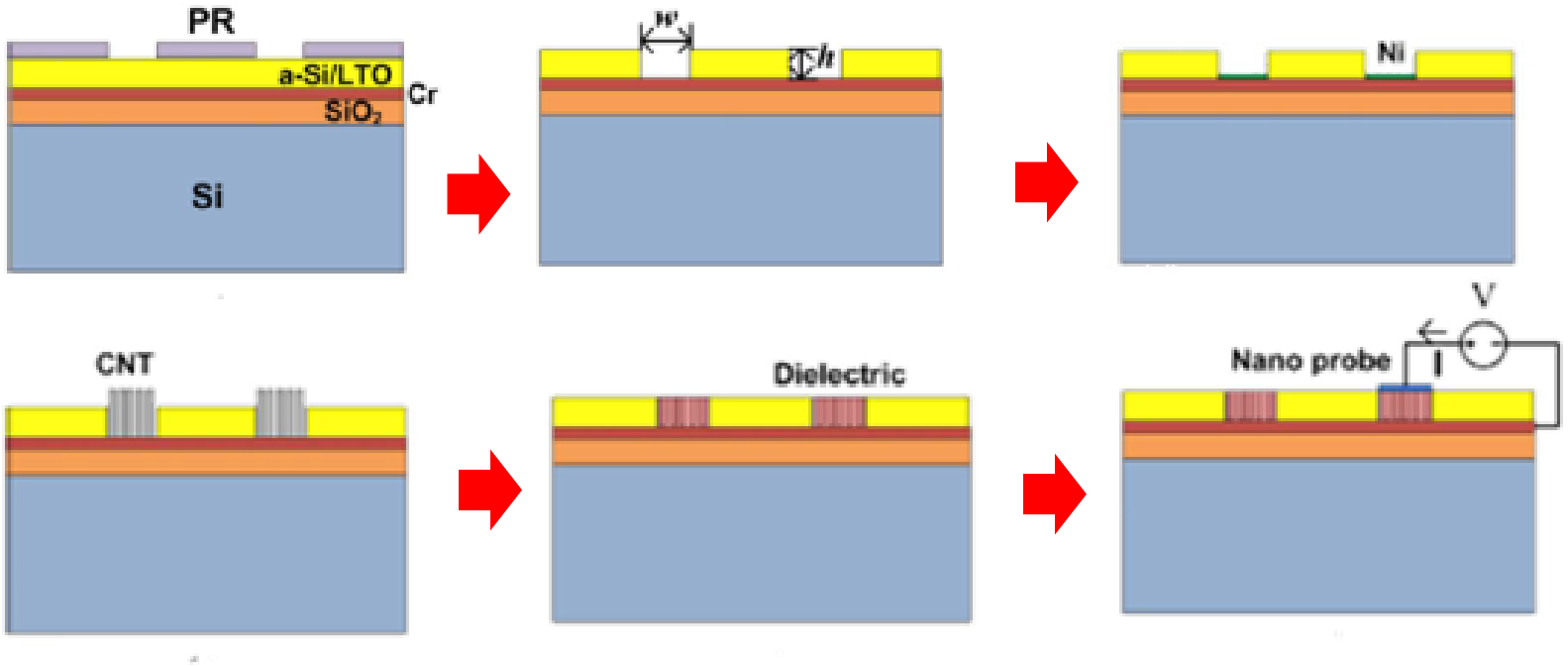
CNT Vias - Objectives

- Comprehensive characterization of CNT vias with linewidths approaching those used in current technology node
- Development of technique to extract contact resistance of CNT vias with linewidths down to 40 nm
- Assessment of CNT via performance and reliability and compare with Cu and W

Via Test Structure Fabrication

- **Process includes a-Si hard mask for via etching to achieve vertical sidewalls**

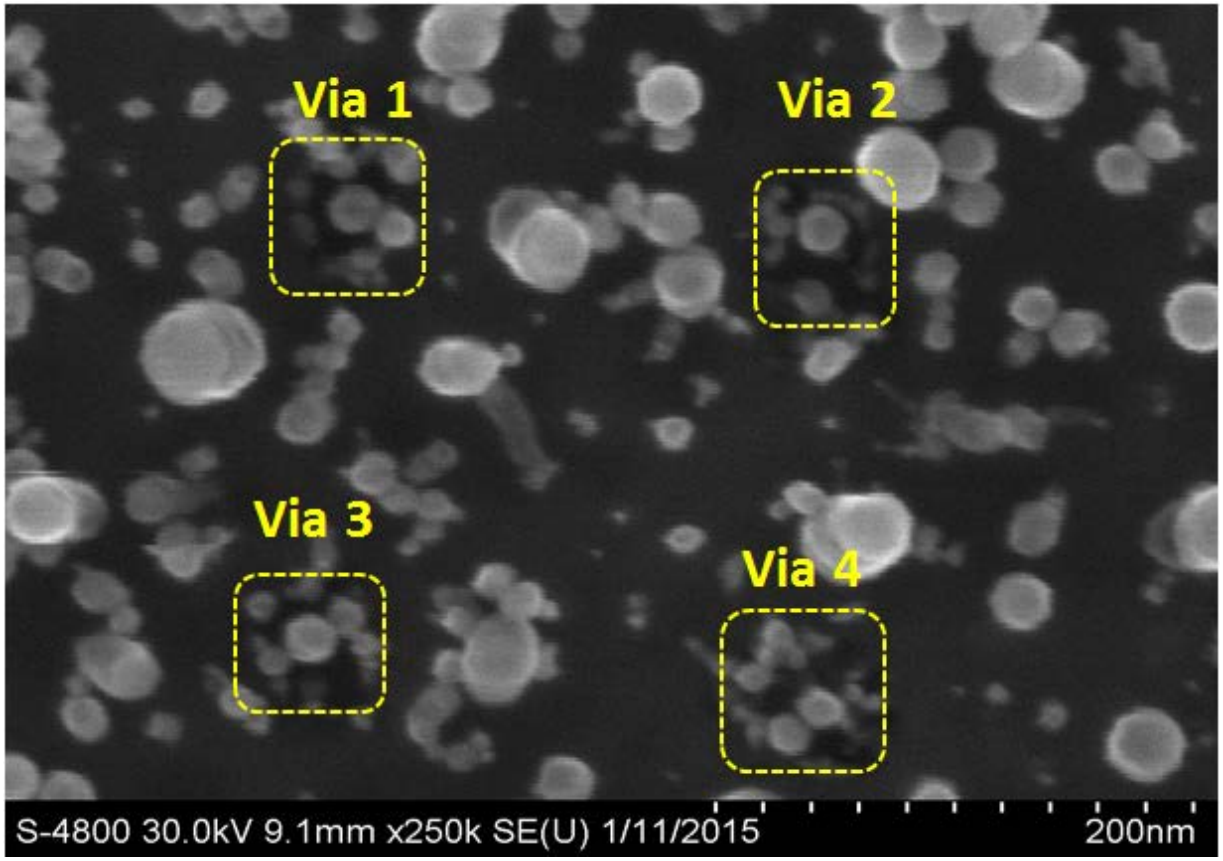




C. Zhou, et al., *IEEE EDL* 36 (2015)

CNT Growth in 60 nm Vias

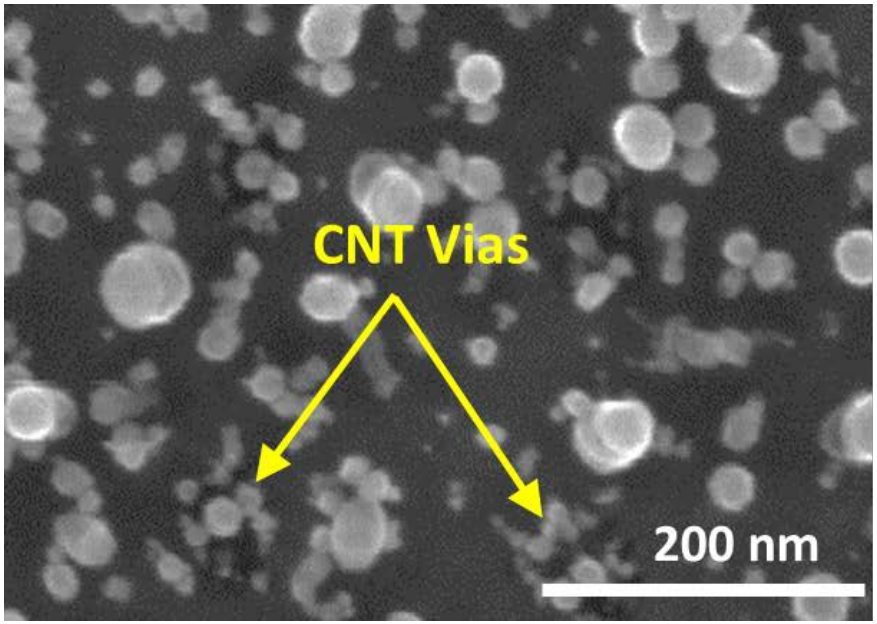
- Vertically aligned CNTs are grown in vias using Ni catalyst in plasma-enhanced chemical vapor deposition (PECVD) system

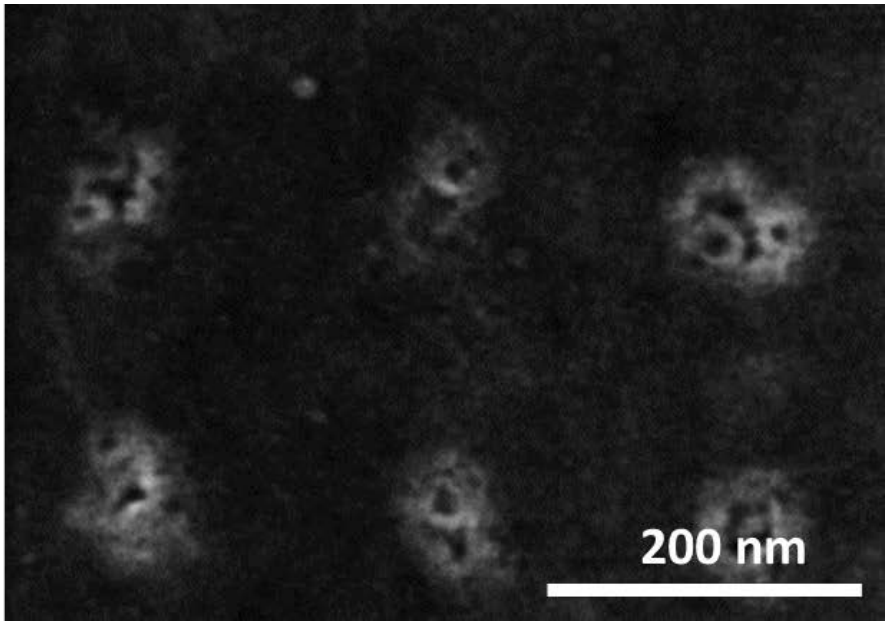


Areal density ~ 2×10^{11} /cm^2 Average CNT diameter ~ 15 nm

Dielectric Filling and Polishing

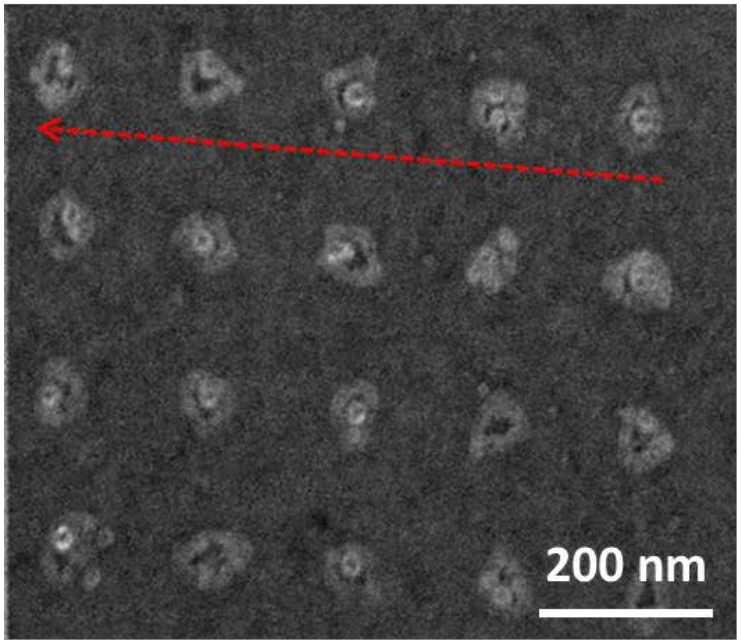
- To maintain CNT vertical alignment in vias and to optimize CNT/metal interface at via top contact, void in via filled with Al_2O_3
- Atomic Layer Deposition of Al_2O_3 using trimethylaluminum and water at a rate of 1 Å/cycle

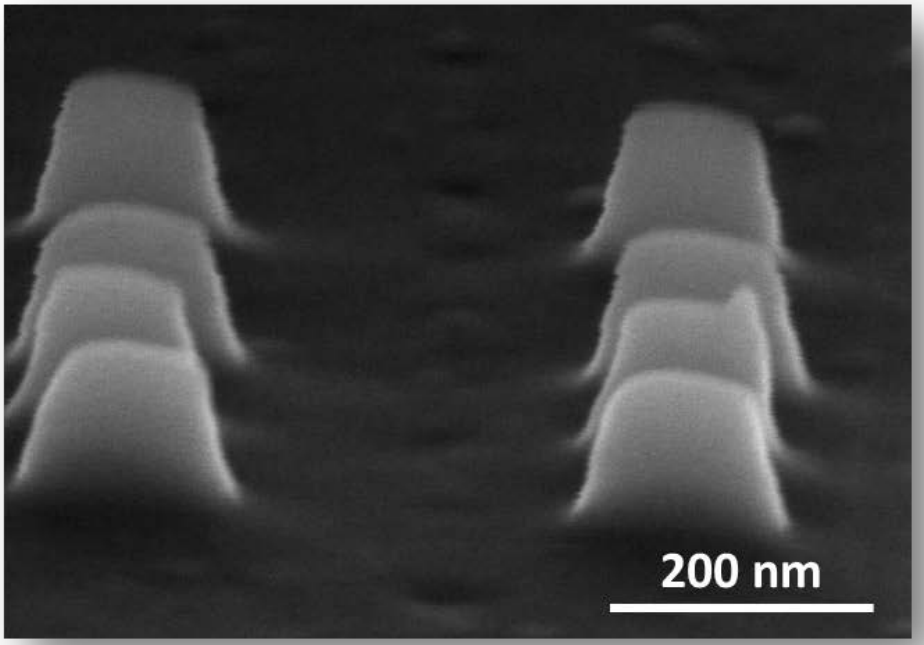




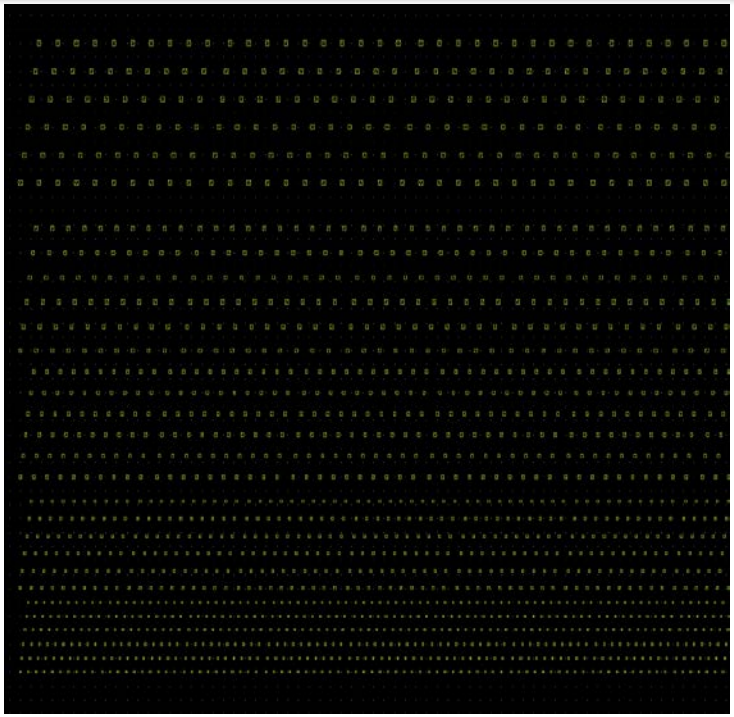
Via Top Contact Metallization

- Selective top-contact metallization using electron-beam-induced deposition (EBID)
- Pt deposited on alternate vias along the wedge for five different via heights

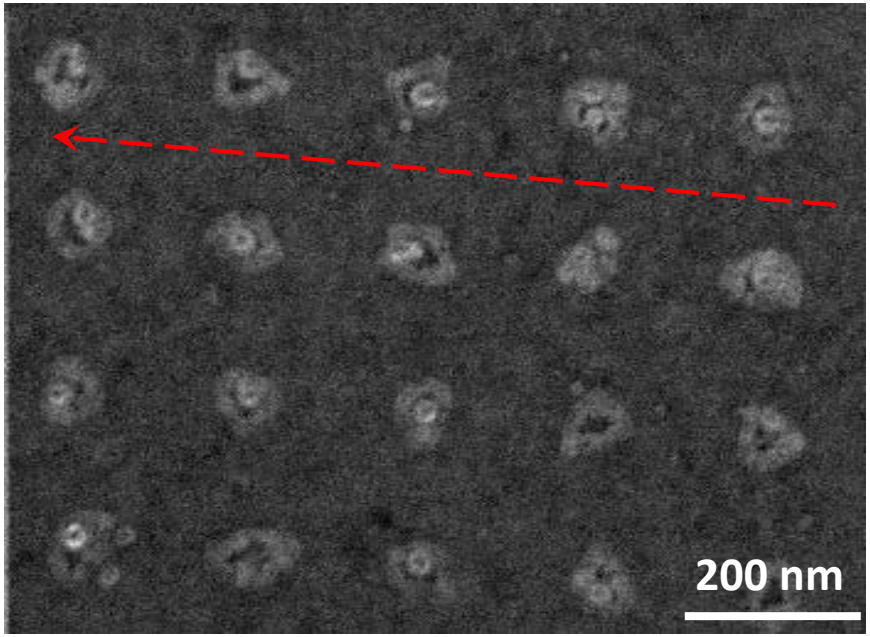




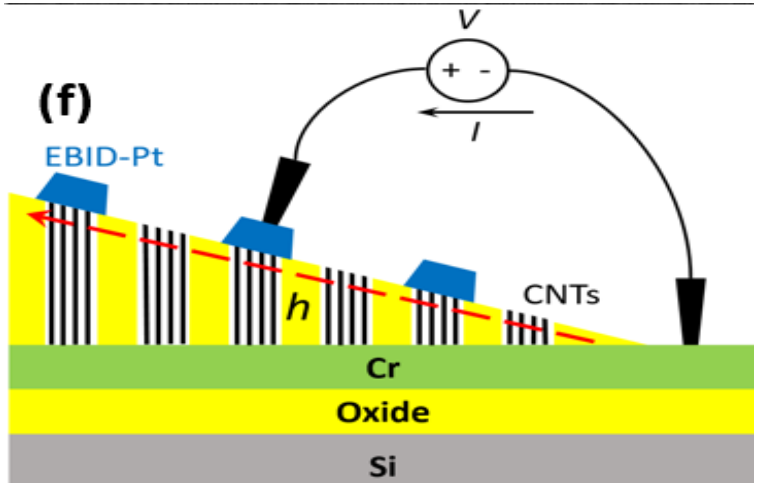
Via Test Structures



CNT via patterns: layout design

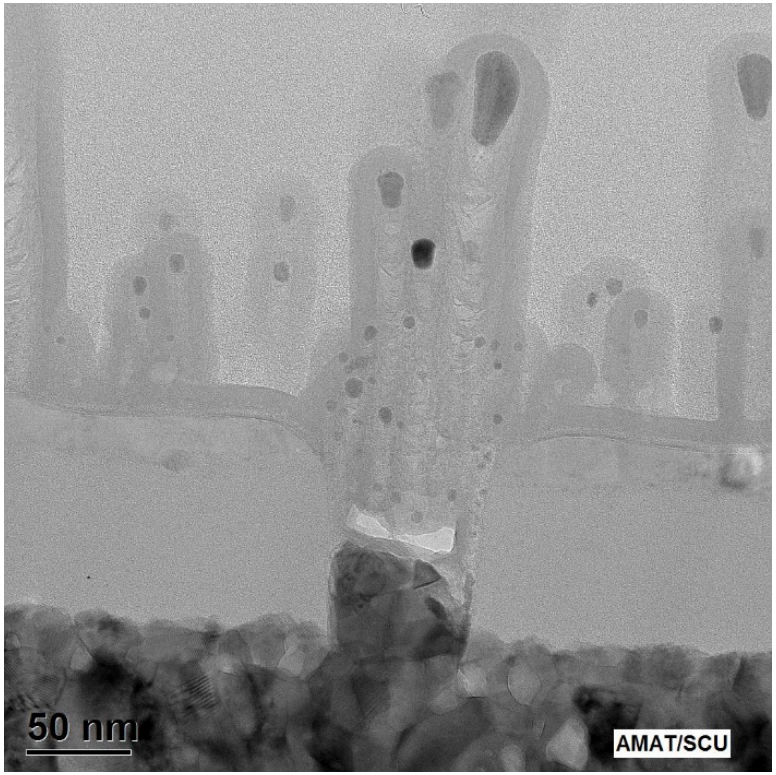


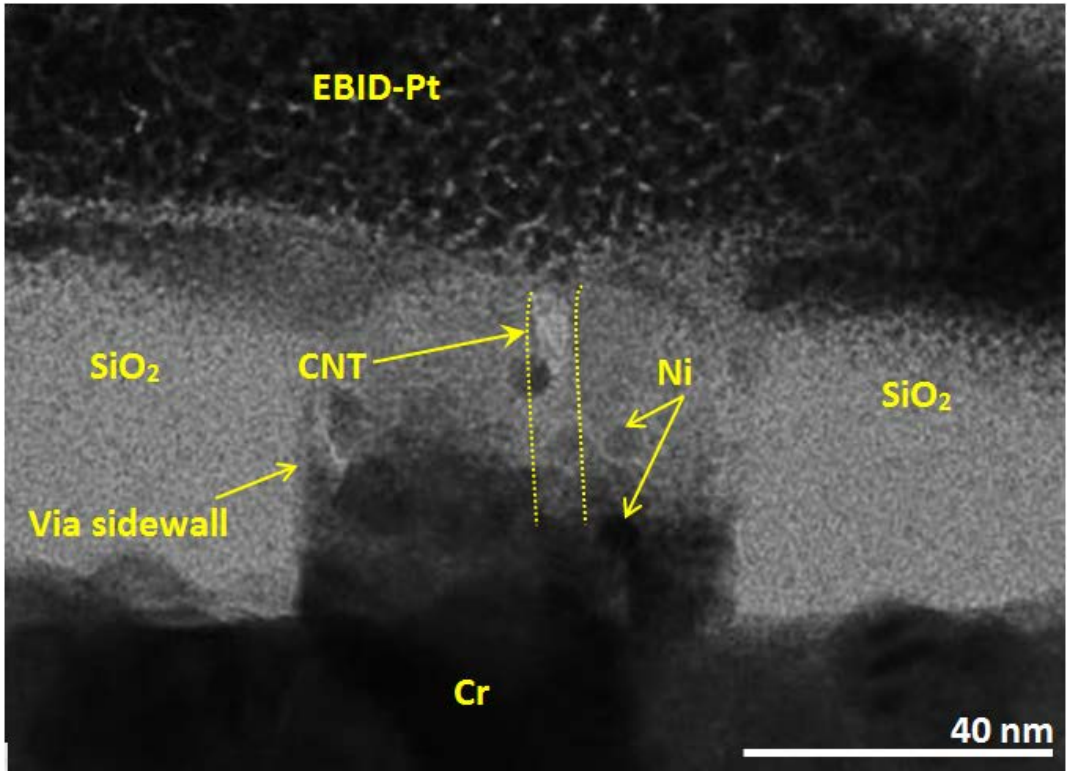
Wedge structure to create multiple heights



Structural Characterization: TEM Imaging

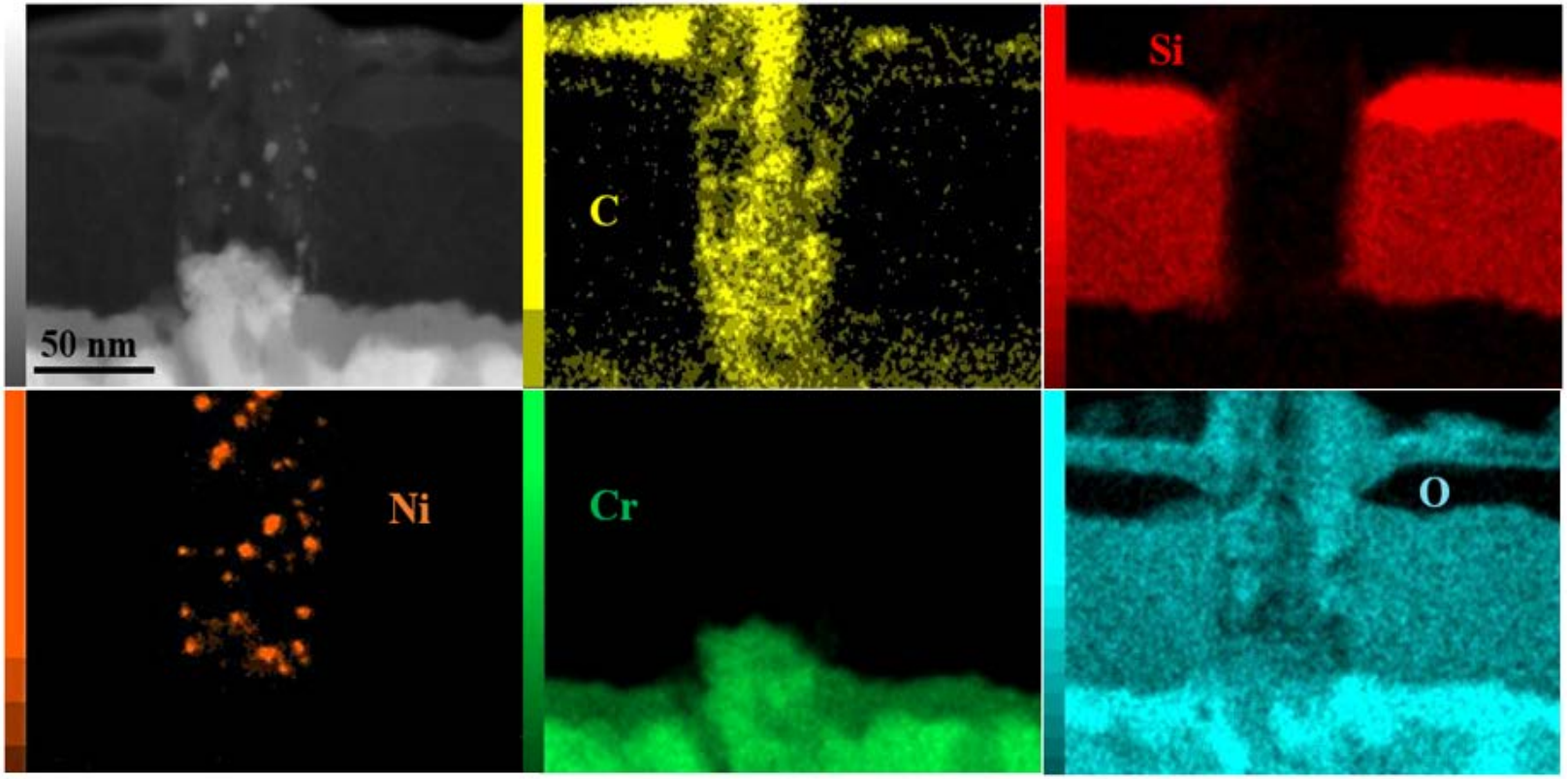
- CNT via near middle of wedge





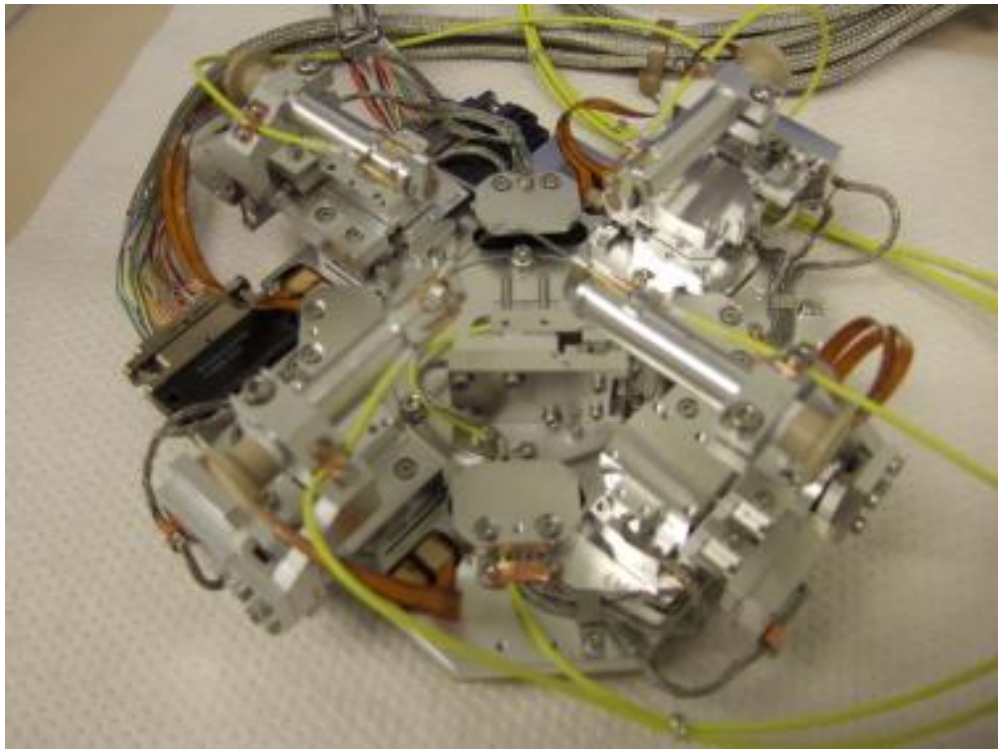
Structural Characterization: EDS Analysis

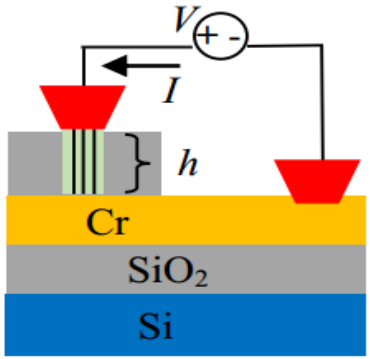
- C signal traced to original CNT-Cr underlayer interface
- No evidence of stray Ni particles reacting with a-Si to form silicide
- Supports CNT length spanning the entire via height

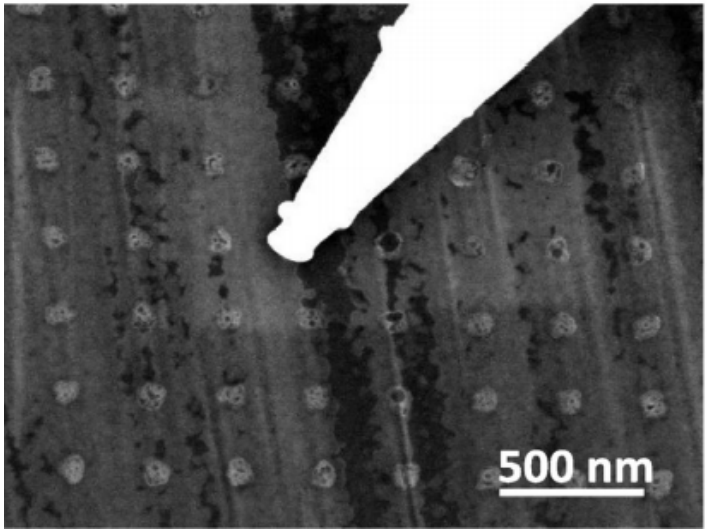


Electrical Characterization

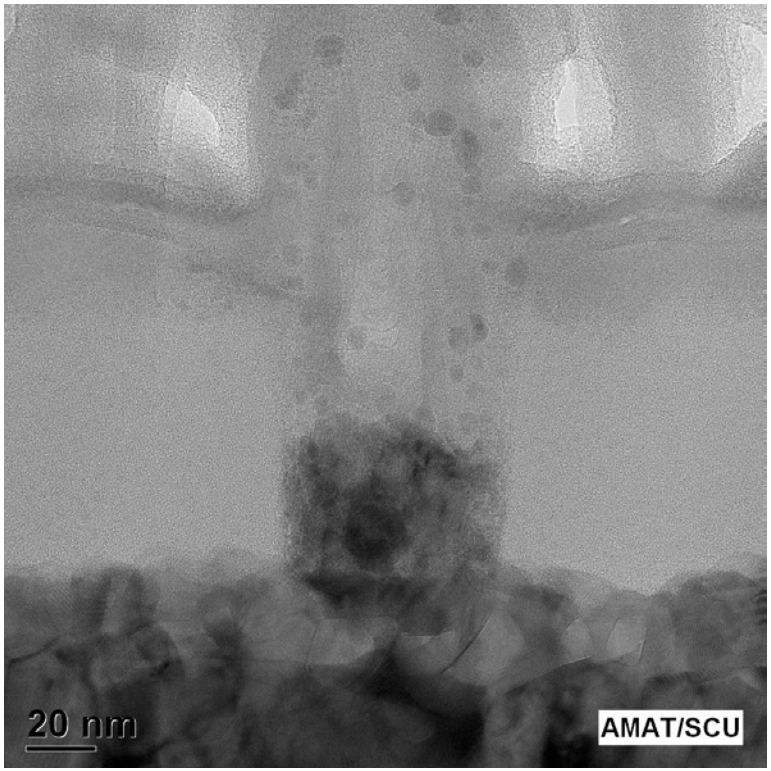
- Nanoprobing on individual vias to measure resistance

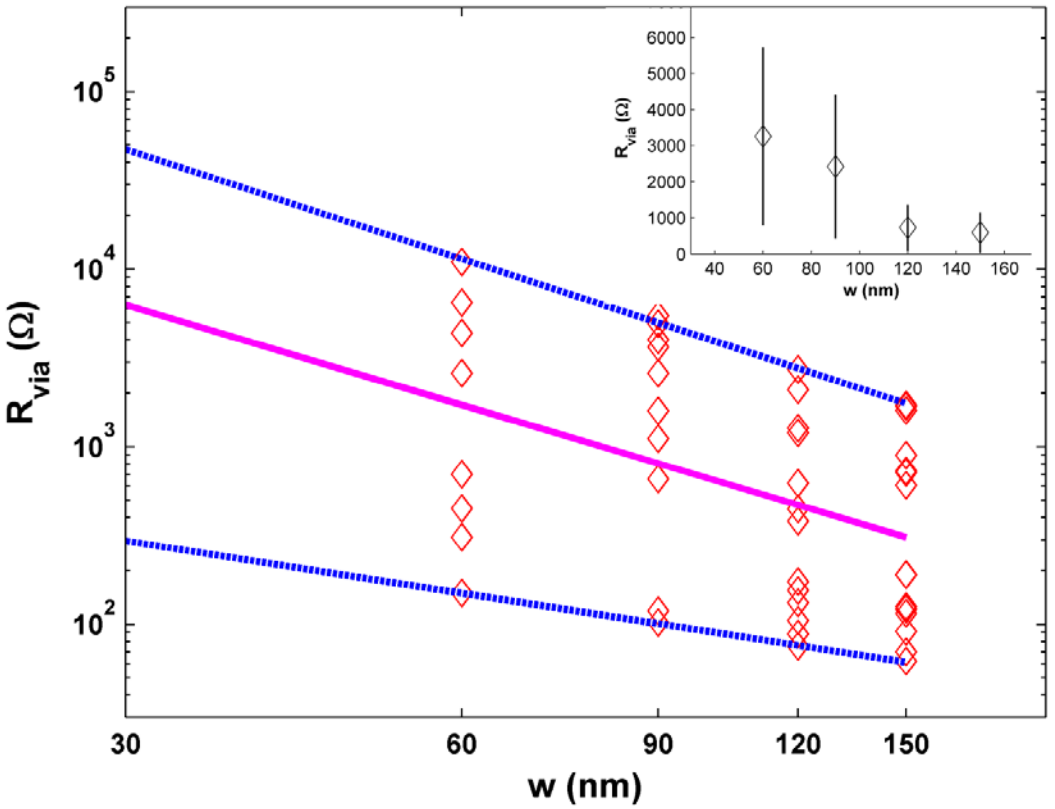






Resistance of CNT Vias





- The lowest resistance obtained for 60 nm via is 150 Ω and the lowest extrapolated resistance for a 30 nm via is 295 Ω, about 5 × that of W.
- Based on the log-log plot, the statistical average R_{via} for 60 nm vias is 1.7 kΩ with standard deviation between 420 Ω and 7.1 kΩ.

Analysis of CNT Via Resistance Data

$$R_{via} = (R_{Cr} + R_{probe} + R_{probe\text{-}Cr}) + (R_{probe\text{-}CNT} + R_{Cr\text{-}CNT}) + R_{CNT}$$

$$\equiv R_m + R_C + R_{CNT}$$

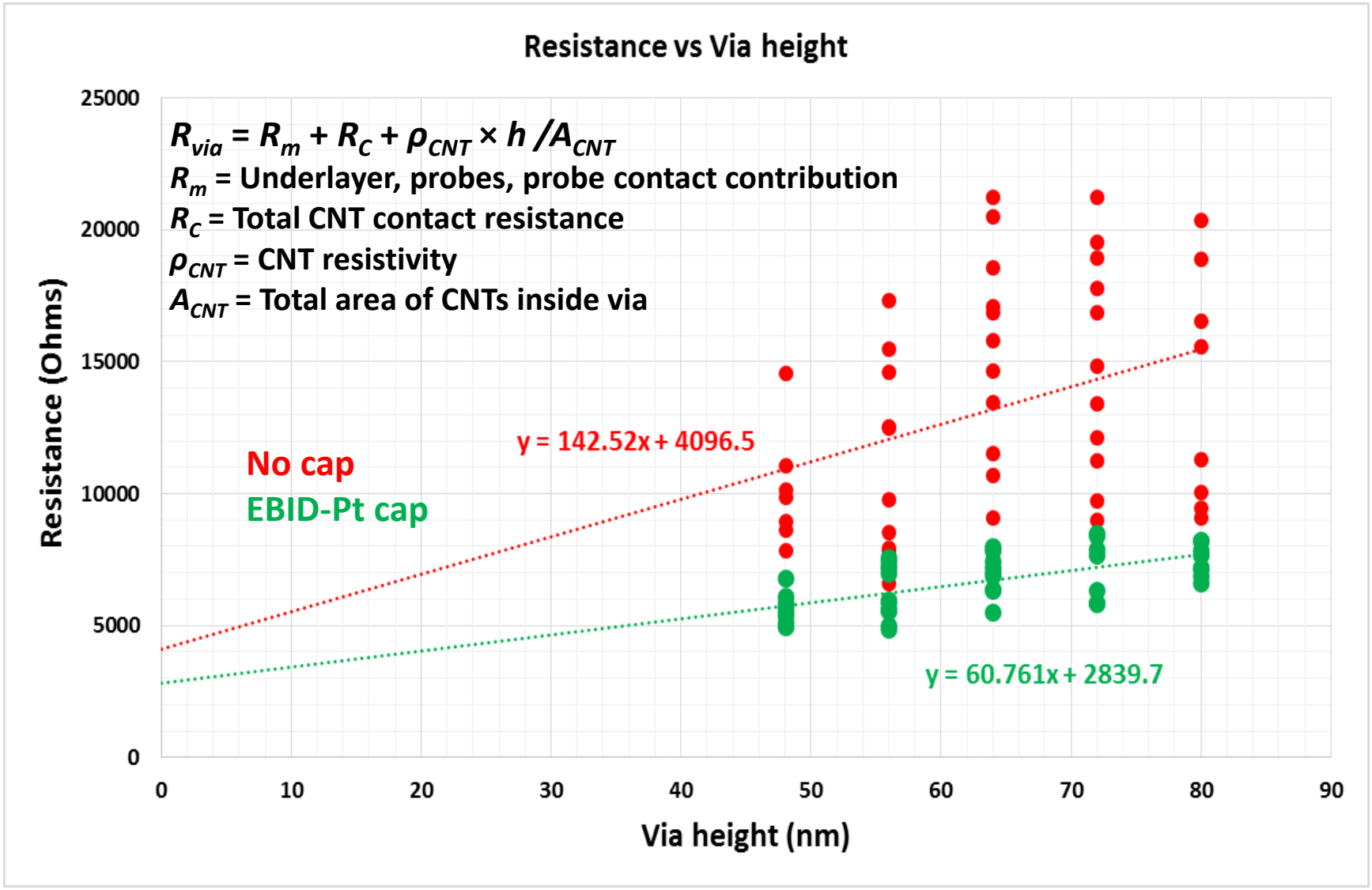
$$= R_m + R_{ci}/(D_{CNT} \times w^2) + \rho_{CNT} \times h/(D_{CNT} \times w^2 \times A_{CNT})$$

- R_m estimated by direct probing of Cr underlayer, ~15 Ω
- R_{ci} is contact resistance of individual CNT

$$\log(R_{via}) \cong \log[R_{ci}/D_{CNT} + \rho_{CNT} \times h/(D_{CNT} \times A_{CNT})] - 2 \times \log(w)$$

- Slope of fitted $\log(R_{via})$ *vs* $\log(w)$ measured data is -1.9!

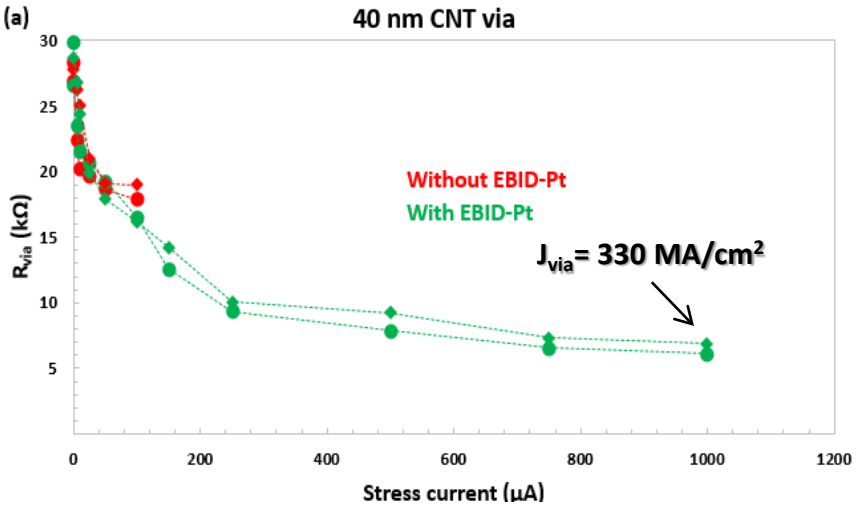
Resistance of 40 nm CNT Vias

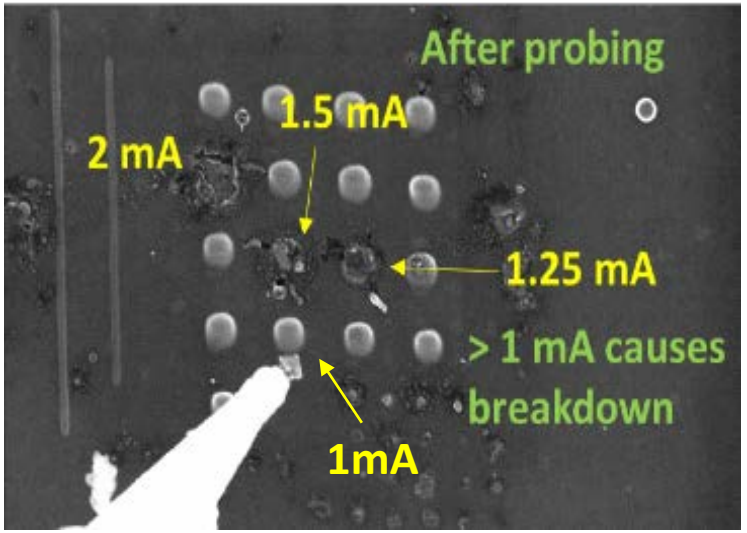


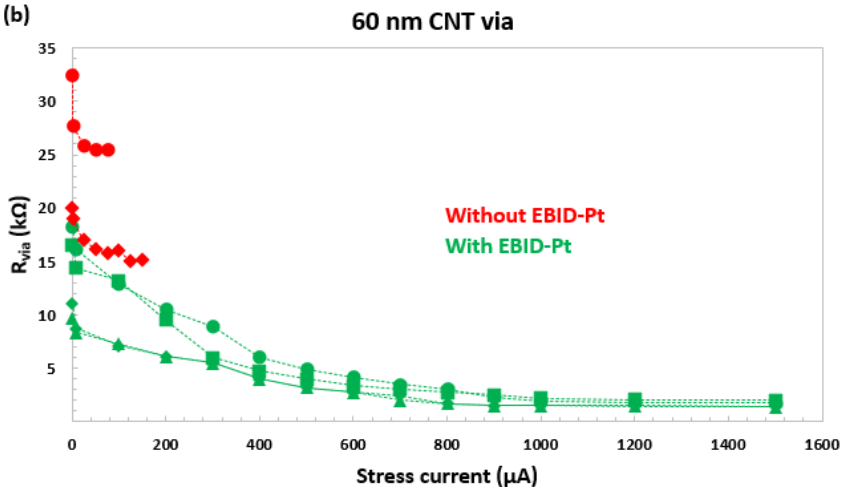
A. Vyas, et al., Nanotechnology,27(37),(2016)

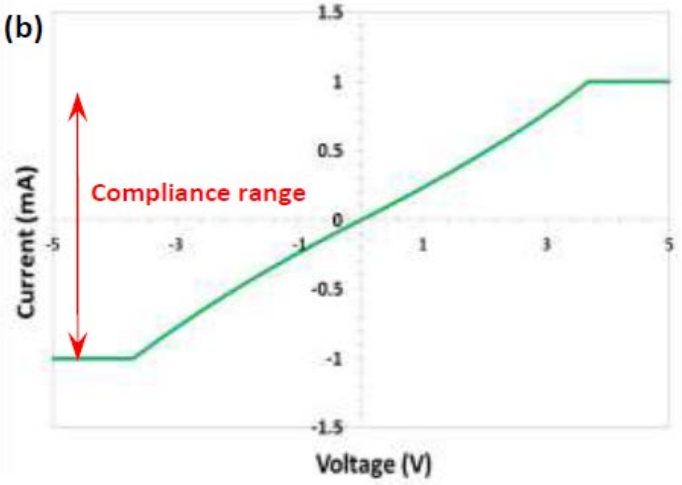
CNT Via Reliability

- Current stress experiment carried out to determine maximum current-carrying capacity









A. Vyas, et al., Nanotechnology, 27(37), 2016

Comparisons with Cu and W

	Via Width × Height	CNT Growth Temp (˚C)	CNT Areal Density (#/cm^2)	Average CNT diameter (nm)	R_{via} (kΩ)	J_{via} (MA/cm^2)
This Work	**40 nm × 80 nm**	**700**	**10^{12}**	**9**	**6.1**	**330**
CNT via (Graham 2005)	30 nm × 150 nm	700	1.5×10^{11}	15	7.8	400
CNT via (Katagiri 2011)	70 nm × 100 nm	450	5×10^{11}	10	11	100
Cu (Adelman 2014)	30 nm × 130 nm	NA	NA	NA	0.025	2.5
W (Walls 1997)	30 nm × 130 nm	NA	NA	NA	0.060	1

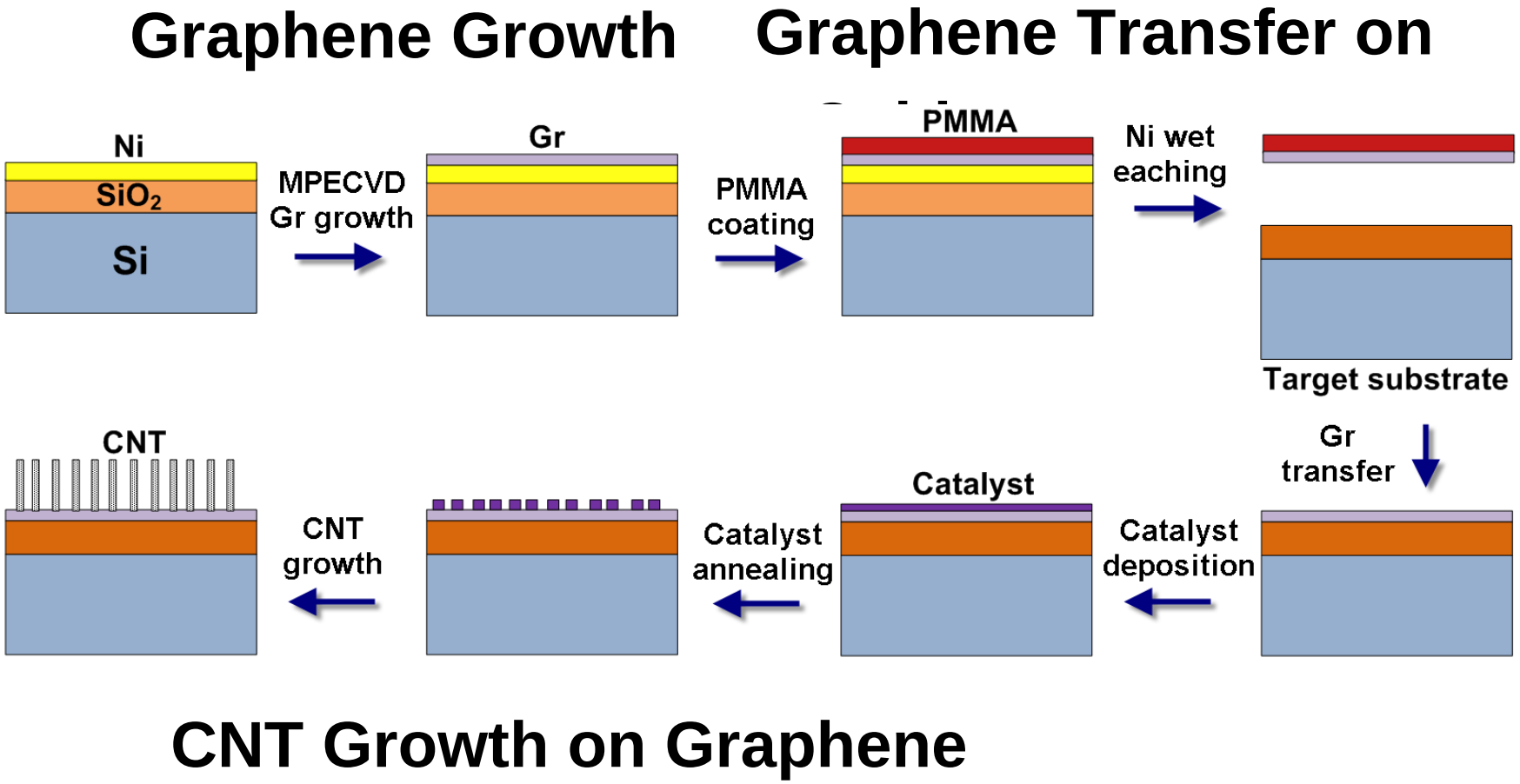
Summary of CNT Via Results

- CNT vias down to 40 nm width fabricated and characterized
  - "Best" projected resistance for 30 nm CNT via ~ 5 x W via resistance
  - Current capacity ~ 300 MA/cm^2
- Ongoing efforts to decrease CNT diameter and increase CNT packing density to reduce via resistance
- Additional contact engineering needed to reduce overall resistance
- Further considerations on contact resistance reduction with CNT growth process improvements

Outline

- Introduction
  - Scaling in Integrated Circuits
  - Interconnects versus Transistors
- CNT as 1D Interconnect Structure
- **CNT-Graphene for All-Carbon 3D Interconnects**
- Summary

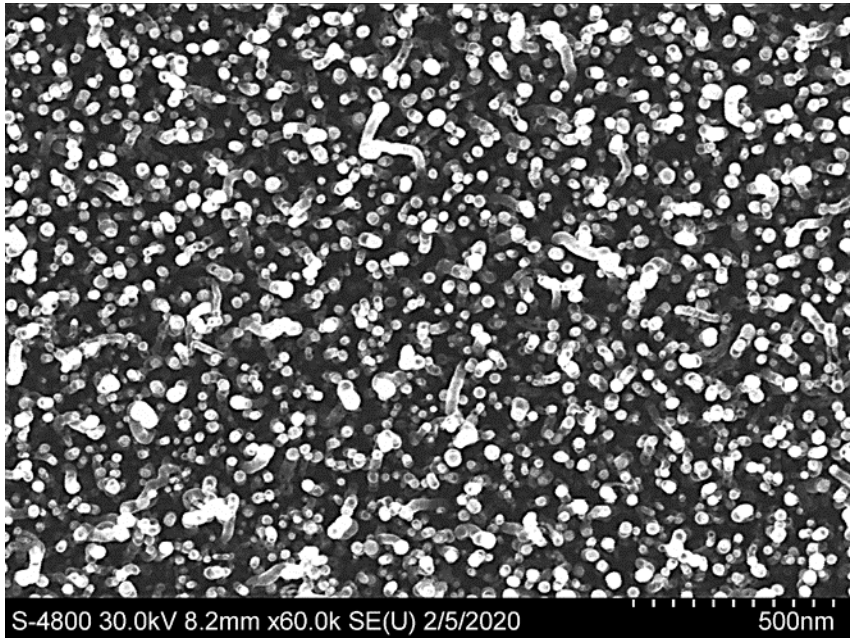
CNT/Graphene Test Structure Fabrication

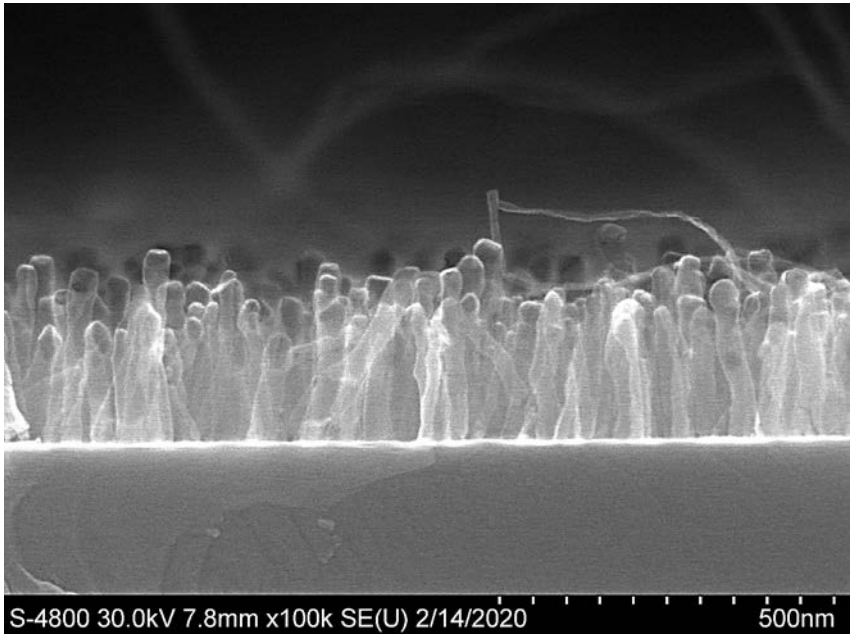


C Zhou, et al., *Nanotechnology* 28 (2017)

CNT grown on Graphene

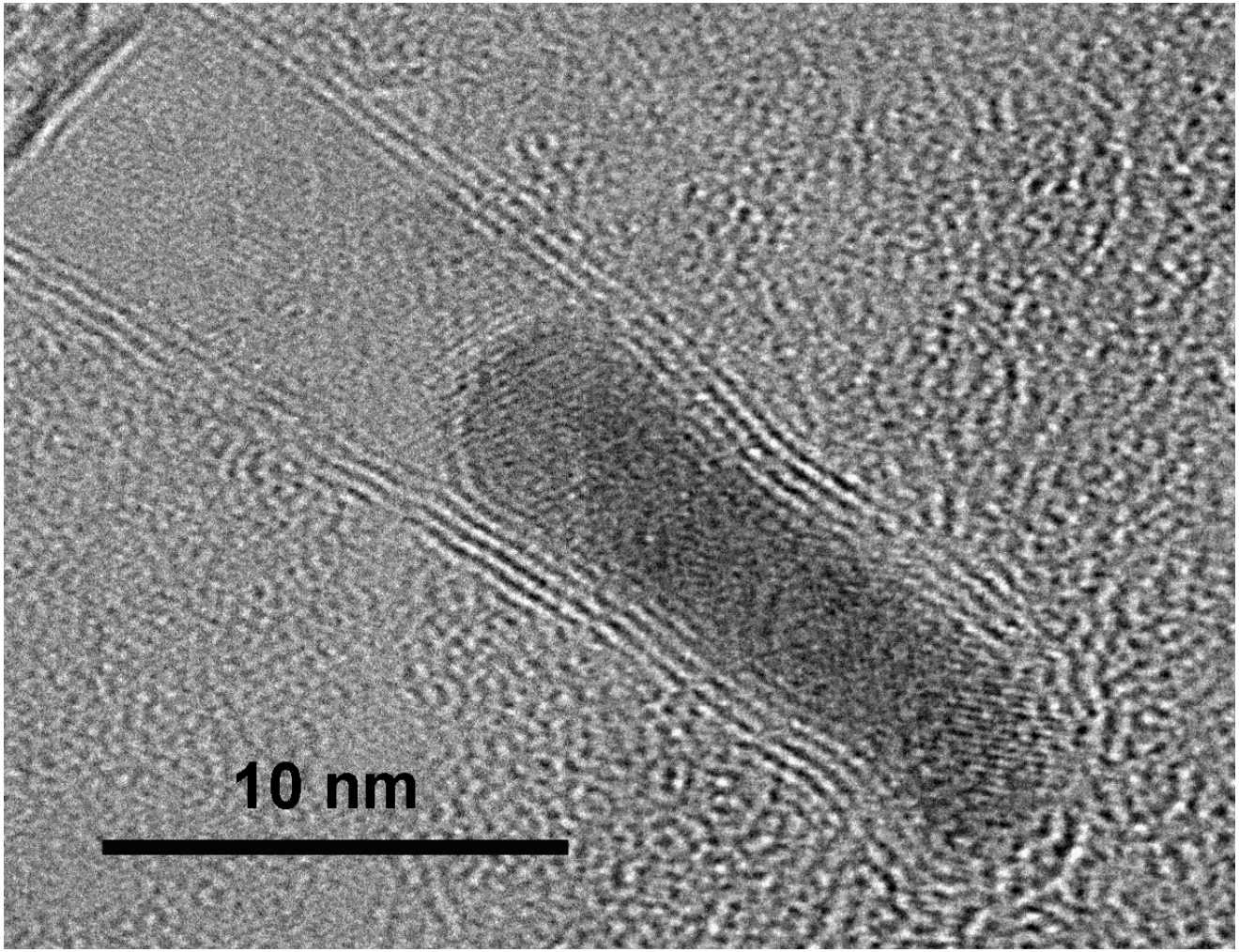
Ni catalyst





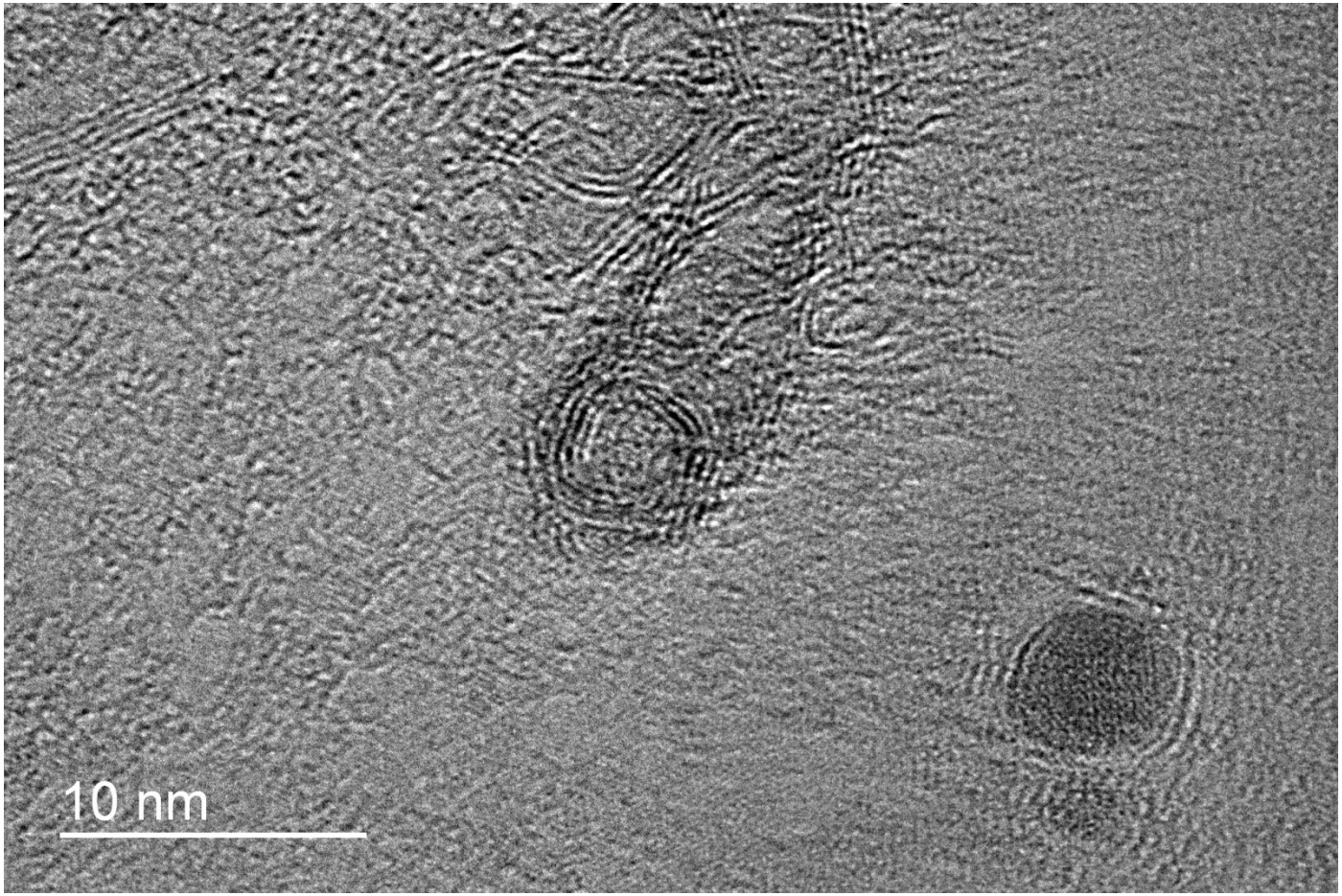
CNTs grown with PECVD at 800VDC on MLG using Ni catalyst

CNT/Graphene: TEM Characterization



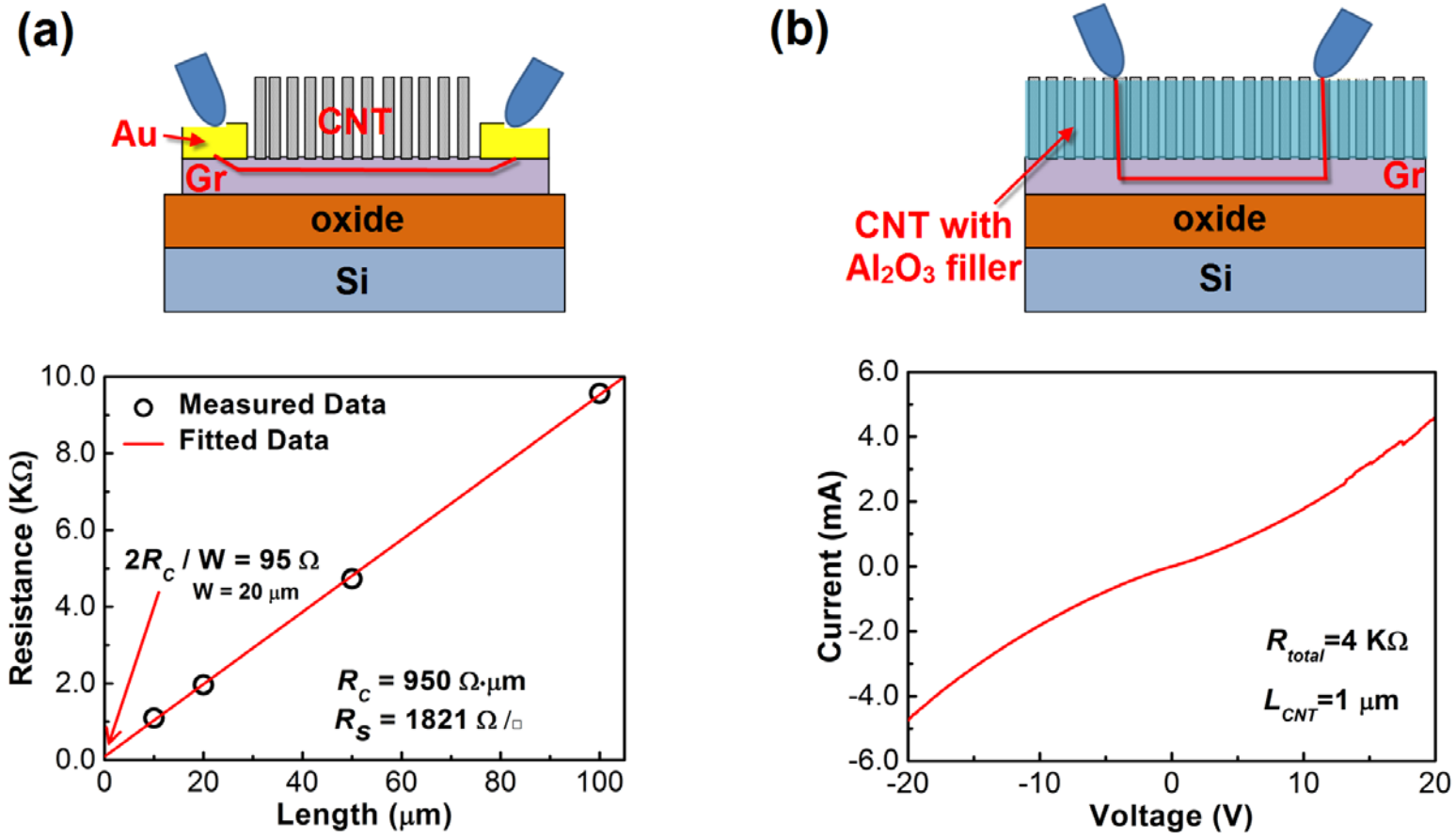
CNT: tip growth mode

CNT/Graphene: TEM Characterization



CNT cross-section revealed by TEM imaging

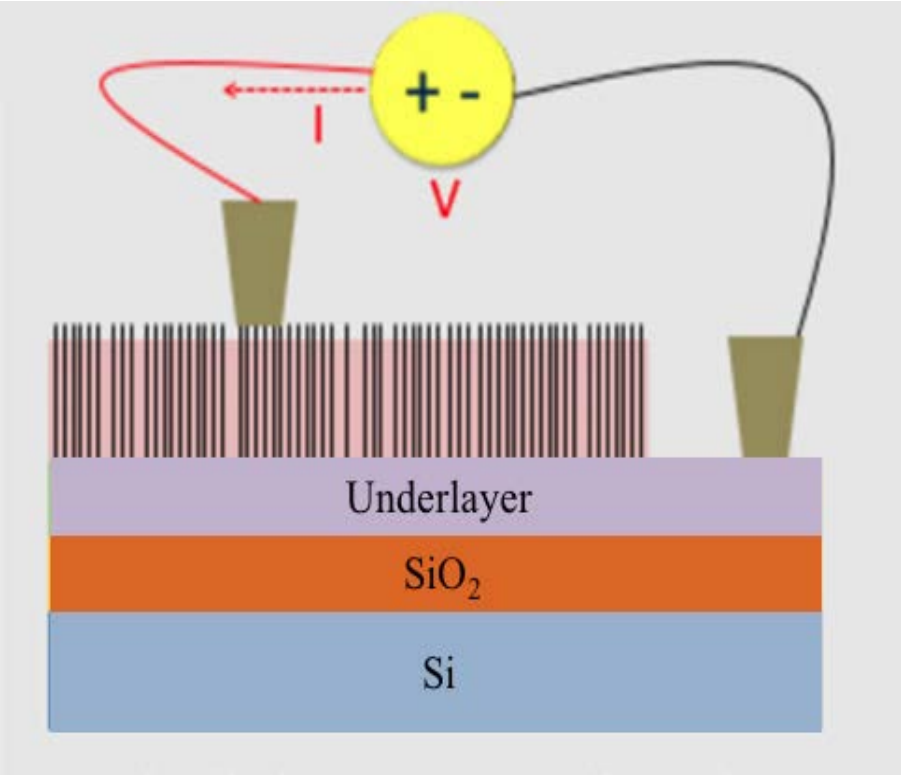
Electrical Characterization



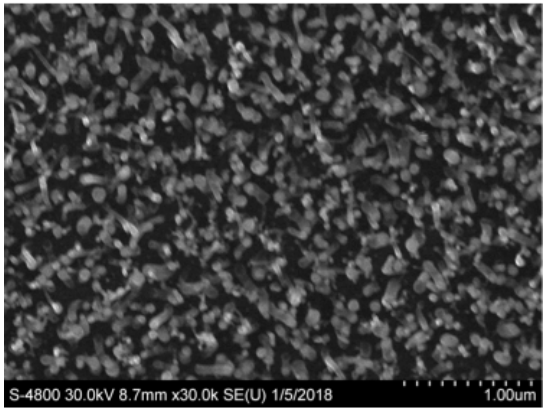
- **ALD oxide filler to strengthen CNT forest**
- **Exposure of CNT tips for probe contact**
- **CNT/Graphene contact resistance extraction in progress**

Electrical Characterization

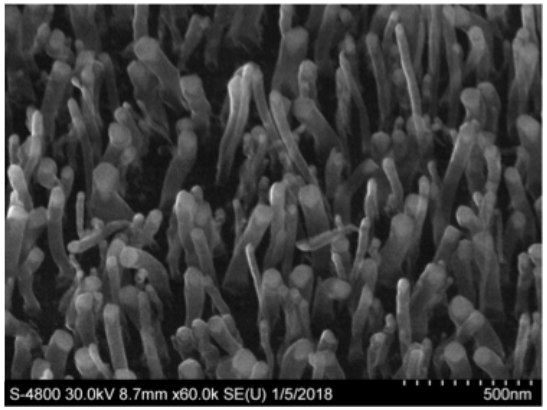
- Ground probe fixed on graphene while bias probe lowered at small increments to ensure direct contact with CNTs.
- Nanoprobing enhances the probability of making direct contact with CNTs.



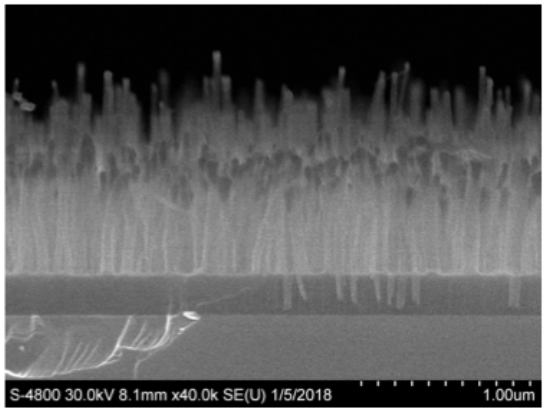
Aligned CNTs Grown on Graphene



Top-view SEM image of 800VDC PECVD-grown CNT/MLG.



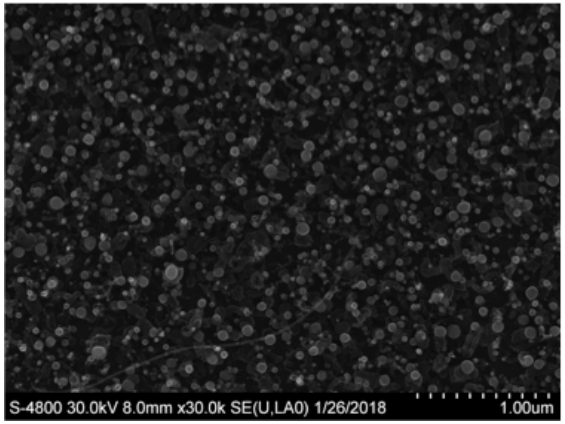
Tilted-view SEM image of 800VDC PECVD-grown CNT/MLG.



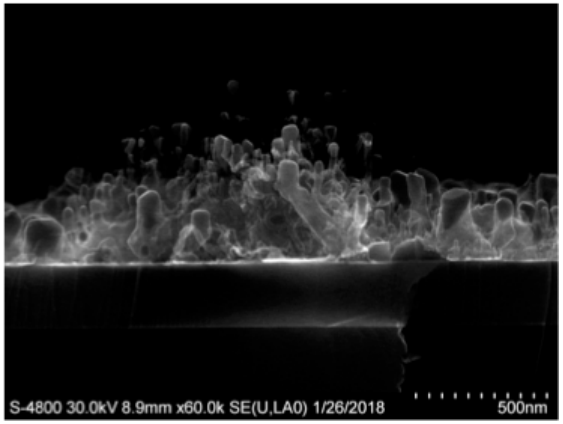
Side-view SEM image of 800VDC PECVD-grown CNT/MLG.

- CNTs grown on MLG using PECVD at 800VDC show vertical alignment.
- However, the structure is not conductive due to plasma damage to MLG underlayer.

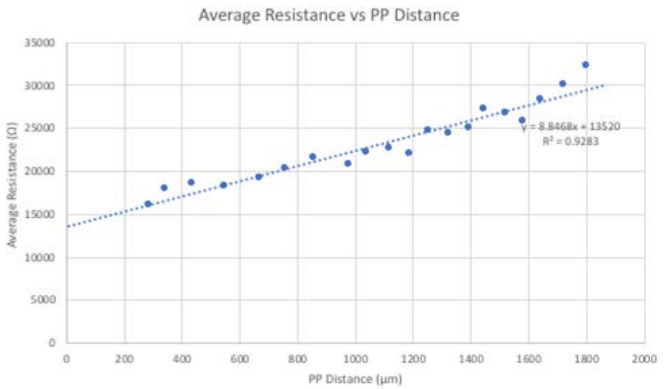
CNTs Grown on Graphene using PECVD at 500VDC



Top-view SEM image of 500VDC PECVD-grown CNT/MLG.



Side-view SEM image of 500VDC PECVD-grown CNT/MLG.

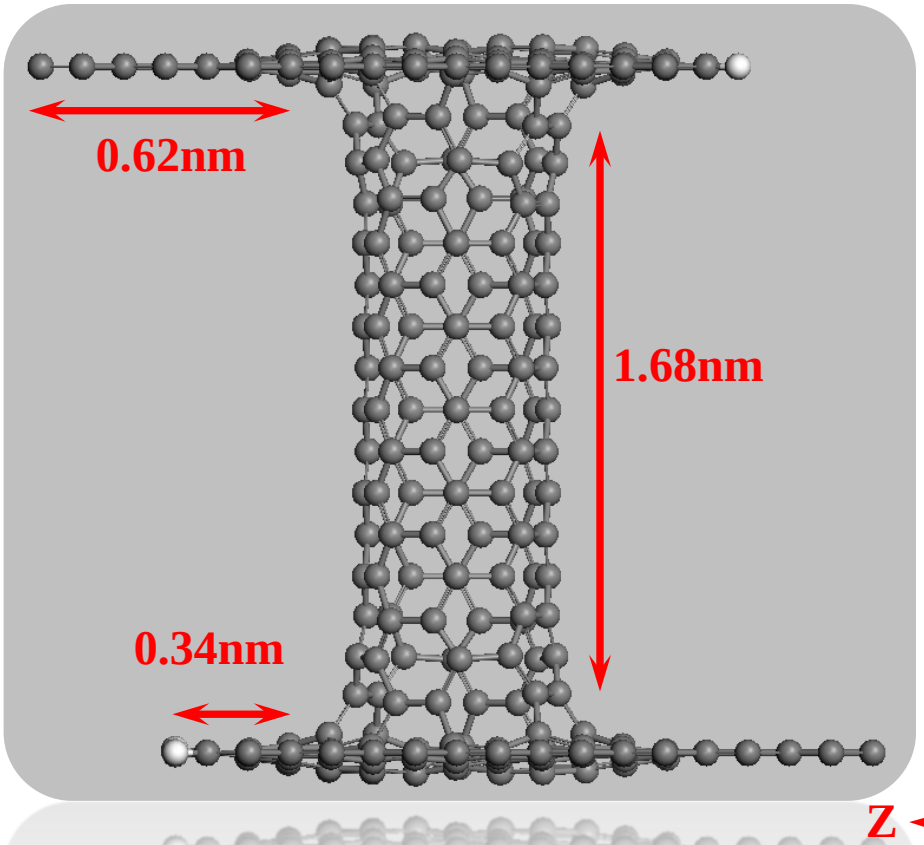


Average resistance vs PP distance for CNT/MLG sample grown using 500VDC PECVD.

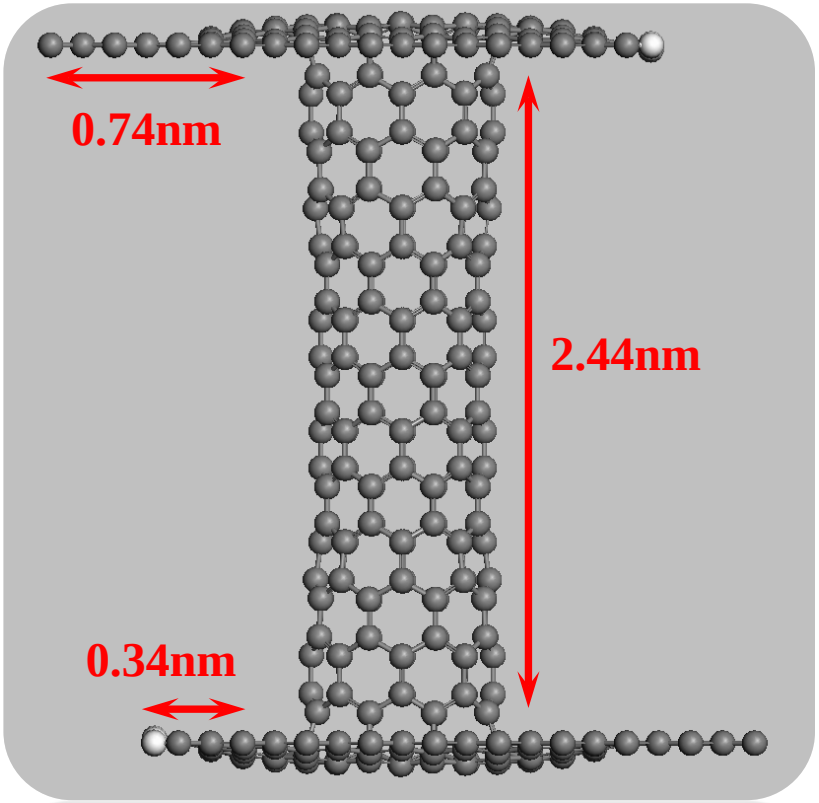
- I-V and resistance results show conduction with higher overall resistance than that of plain MLG, with bias probe probably making partial contact with graphene.
- CNTs not as well aligned as those obtained using 800VDC, but improved alignment over those with thermal CVD.
- Reduced DC voltage in PECVD appears to preserve MLG underlayer.

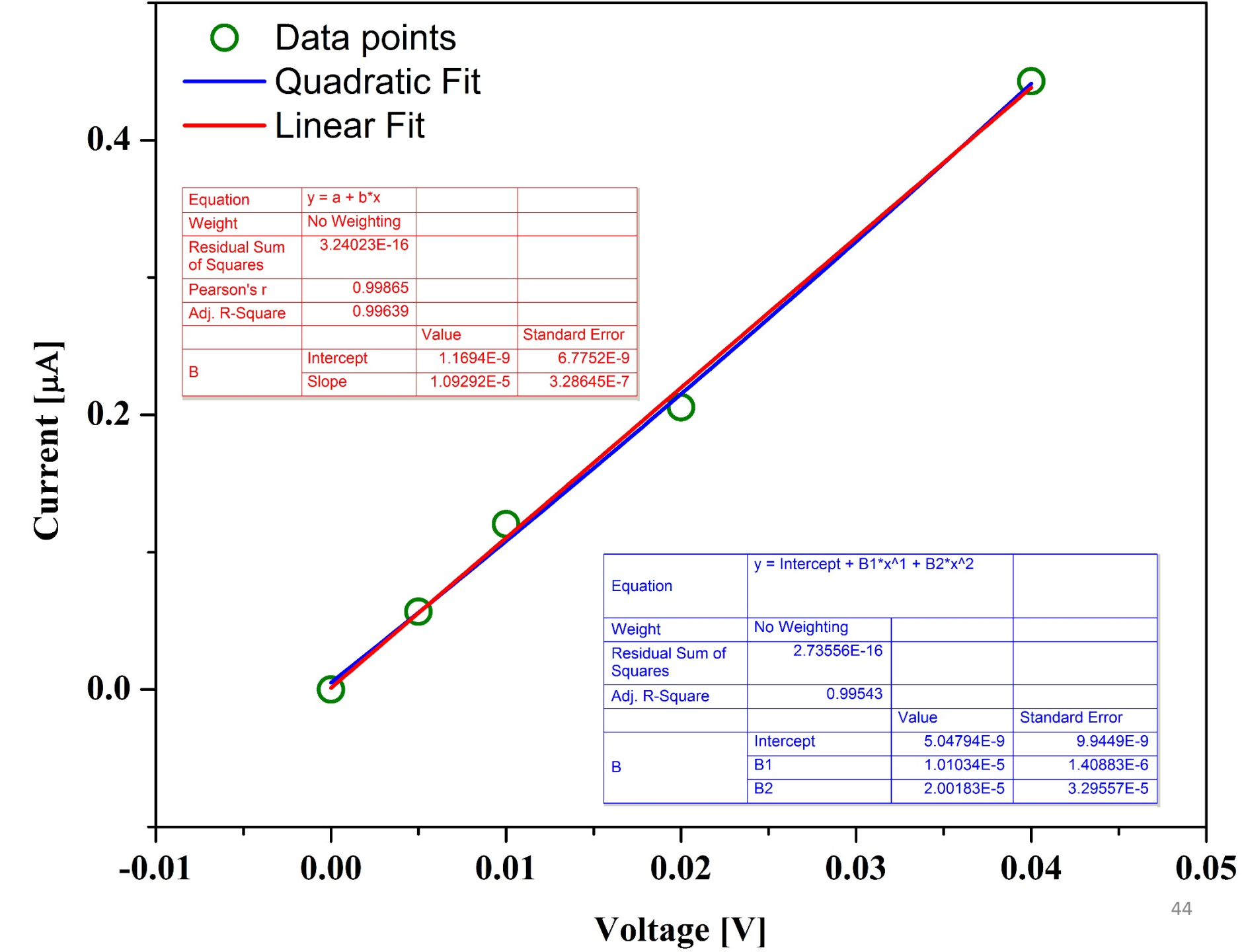
First-Principles Study of CNT/Graphene

112 atoms of CNT , 536 total atoms
(4,4) CNT radius = 0.542nm



192 atoms of CNT , 572 total atoms
(8,0) CNT radius = 0.626nm




Data points
Quadratic Fit
Linear Fit
Current [μA]
0.4
0.2
0.0
-0.01
0.00
0.01
0.02
0.03
0.04
0.05
Voltage [V]
Equation y = a + b*x
Weight No Weighting
Residual Sum of Squares 3.24023E-16
Pearson's r 0.99865
Adj. R-Square 0.99639
Value Standard Error
B Intercept 1.1694E-9 6.7752E-9
B Slope 1.09292E-5 3.28645E-7
Equation y = Intercept + B1*x^1 + B2*x^2
Weight No Weighting
Residual Sum of Squares 2.73556E-16
Adj. R-Square 0.99543
Value Standard Error
B Intercept 5.04794E-9 9.9449E-9
B B1 1.01034E-5 1.40883E-6
B B2 2.00183E-5 3.29557E-5

Summary on CNT/Graphene

- CNT/Graphene test structure successfully fabricated
- Graphene remains intact after sputtering and CNT growth
- CNT cross-section is observed using TEM, suggesting possible bonding between CNT walls and graphene surface prior to sample preparation
- Further work on CNT growth on graphene with varying process parameters and contact resistance extraction
- First-principles calculations on CNT/Gr structure in progress

Acknowledgements

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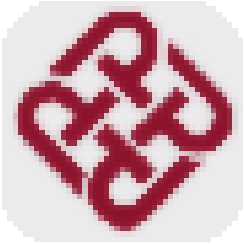
Yihan Chen, Zubair Ahmed, Salahuddin Raju, Mansun Chan



Chai Yang

Phillip Wang