Resistance Determination for Sub-100-nm Carbon Nanotube Vias

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***Abstract*— We report resistance results from carbon nanotube (CNT) vias of widths from 150 to 60 nm for potential application in integrated circuits technology. Selective CNT growth inside the vias with an areal density of $2 \times 10^{11}/cm^2$ is achieved with a statistical average resistance of 1.7 kΩ with standard deviation between 420 Ω and 7.1 kΩ, and lowest resistance of 150 Ω for 60 nm vias, the lowest reported value for sub-100 nm-CNT vias. Statistical analysis yields a best-case projected value of 295 Ω for a 30 nm via, within one order of magnitude of its copper and tungsten counterparts.**

***Index Terms*— Carbon nanotube (CNT), interconnect, via.**

I. Introduction

As THE minimum feature size of integrated circuit (IC) technology continues to shrink, current interconnect materials such as copper (Cu) and tungsten (W) are rapidly approaching their scaling limit due to increasing resistivity and inability to withstand high current densities. Carbon nanotube (CNT) has been investigated extensively as a candidate for future on-chip interconnects due to its much higher current-carrying capacity than those of Cu and W, low resistance, and scalability down to end-of-roadmap IC technology nodes [1]. However, there are still numerous technical challenges to be addressed before CNTs can be utilized in future IC technologies. An interconnect via containing densely packed vertically aligned CNTs with resistance comparable to that of Cu is still not within reach [2]. And achieving low contact resistance between CNT and metal electrodes continues to be a daunting challenge [3]. Efforts on increasing the CNT areal density and decreasing the CNT diameter, as well as improving the CNT-metal contact resistance and process compatibility have made CNT more attractive as the next-generation interconnect material [2]–[7]. To study the potential of CNT vias for future technology nodes, it is important to examine the trend for sub-100nm via performance as the downward scaling of feature size continues. Toward this end, we report measured resistance results on fabricated CNT vias with widths (w) from 150 nm to 60 nm. Selective CNT growth in pre-patterned vias is achieved, and statistical analysis of measured resistance versus via width yields a best-case CNT via resistance only five times that of its W counterpart.

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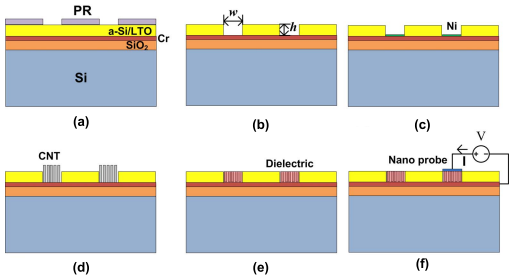

Fig. 1. Schematic of on-chip CNT via fabrication process. (a) Via patterning. (b) Dry etching and PR removal. (c) Catalyst deposition and polishing. (d) CNT growth. (e) Dielectric filling and polishing. (f) Electrical characterization.

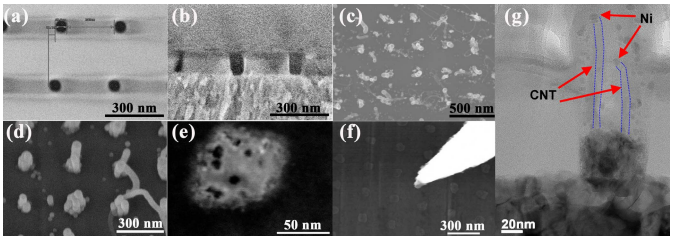

Fig. 2. SEM images of 60 nm vias: (a) top-view image after via patterning; (b) cross section image after dry etching; (c) top-view image of as-grown CNT vias; (d) 30° angled view image of CNT vias after dielectric filling; (e) top-view of a single CNT after ion milling at glancing angle; (f) nanoprobe landing on single CNT via, making direct contact with CNT tips without prior contact metallization; (g) TEM images of a 60 nm CNT via before ion milling, where Ni catalyst particle at CNT tip is indicated by red arrow and the CNT sidewalls by blue dotted lines.

II. Experimental

Fig. 1 presents the process flow for fabricating and characterizing on-chip CNT vias, while Figs. 2(a) to 2(f) show the SEM images at different stages of the process. Starting with a 100 mm SiO_2/Si wafer, a 300 nm chromium (Cr) film is evaporated and then annealed at 400 °C to achieve a smoother surface. Next, a 90 nm low-temperature SiO_2 (LTO) and a 50 nm amorphous Si (a-Si) films are formed by plasma-enhanced chemical vapor deposition (PECVD). E-beam lithography is used to pattern the vias with square cross-sections and widths of 150, 120, 90, and 60 nm [see Fig. 2(a)]. During dry etching, the e-beam resist is first used as a mask for a-Si etching, and then the a-Si thin film is used as the hard mask for SiO_2 etching. After dry etching, vias with vertical sidewalls are achieved [see Fig. 2(b)].

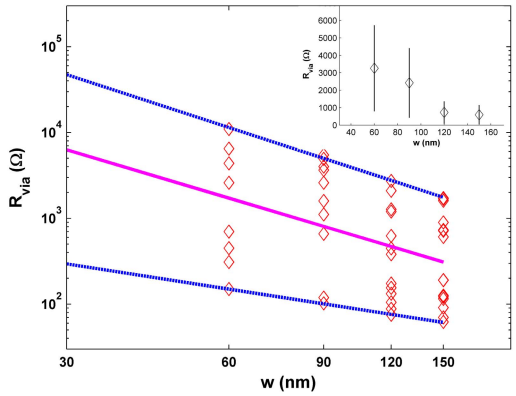

Fig. 3. Measured CNT via resistance versus via width (data points) and statistical linear regression fit of the measured data (solid line). The slope of the fitted line is −1.9, compared to the ideal case of −2. The dash lines show the fits based on the lowest and highest resistances, respectively, for each width. The lowest resistance obtained for a 60 nm via is 150 Ω and the lowest extrapolated resistance for a 30 nm via is 295 Ω. Based on the log-log plot, the statistical average R_{via} for 60 nm vias is 1.7 kΩ with standard deviation between 420 Ω and 7.1 kΩ. As a comparison, the inset shows the arithmetical mean (data point) and standard deviation (vertical bar) for each via width.

Upon deposition of a 4 nm Ni film, the excess Ni outside the vias is removed to ensure selective CNT growth inside pre-patterned vias only [see Fig. 2(c)]. After CNT growth by PECVD at 700 °C, for dielectric filling, a 6 nm Al_2O_3 film is formed by atomic layer deposition (ALD) [see Fig. 2(d)], suitable for high-aspect ratio (A/R) structures such as CNTs. Fig. 2(e) shows the top-view SEM image of a single 60 nm CNT via, revealing multiple CNTs. On average, there are about 7, 15, 26, and 40 CNTs inside the 60 nm, 90 nm, 120 nm, and 150 nm vias, respectively, yielding an average CNT density of about 2×10^{11}/cm^2. Current-voltage (I–V) characteristics of individual CNT vias are measured *in situ* using a nanoprobe inside a SEM chamber [see Fig. 2(f)]. The cross-sectional TEM image of a 60 nm via after filling but before polish with ion milling is shown in Fig. 2(g), revealing CNTs of various heights (as indicated by the Ni particles at the CNT tips) grown from the via base and confirming no growth from the sidewalls.

III. Results and Discussion

Current-stressing is used to improve the nanoprobe-CNT and Cr-CNT contacts [3], [4], resulting in via resistance in the kΩ range or less, as given in the resistance versus width plot in Fig.3. With the I–V measurement setup illustrated in Fig. 1(f), the measured resistance of a single CNT via is given by

$$R_{via} = R_{Cr} + R_{probe} + R_{probe-Cr} + R_{probe-CNT} + R_{Cr-CNT} + R_{CNT}. \quad (1)$$

R_{Cr}, R_{probe}, and $R_{probe-Cr}$ denote the resistances of the Cr underlayer, nanoprobes, and the probe-Cr contact resistance, respectively. Their sum R_m is estimated by measuring the resistance between two nanoprobes landed on the Cr underlayer, yielding 15 Ω for a probe-to-probe distance of ∼10 μm. R_{Cr-CNT} and $R_{probe-CNT}$ represent the total contact resistance R_C, and R_{CNT} the CNT intrinsic resistance. Accordingly, the CNT via resistance becomes $R_{via} = R_m + R_C + R_{CNT}$.

To evaluate the contribution of R_C, we use a previously extracted contact resistance between a single 50 nm-diameter CNT and metal, R_{ci}, ∼300 Ω [5]. R_C can then be estimated by dividing R_{ci} by the number of CNTs inside the via making contact with the nanoprobe, which is the product of CNT areal density D_{CNT} (#CNTs/cm^2) and via cross-sectional area w^2, i.e. $R_C = R_{ci}/(D_{CNT} \times w^2)$. Assuming ohmic conduction along the height of each CNT [4], we obtain

$$R_{via} = R_m + R_{ci}/(D_{CNT} \times w^2) + \rho_{CNT} \times h/(D_{CNT} \times w^2 \times A_{CNT}). \quad (2)$$

Here, ρ_{CNT} is the CNT resistivity, h the CNT height, and A_{CNT} the average CNT cross-sectional area inside the via. Fig. 3 shows the R_{via} versus w measurement results for CNT vias with h = 130 nm as determined from cross-sectional SEM images such as that shown in Fig. 2(b). We note that the measured resistances for each via size span between one to two orders of magnitude. Such wide data spread is attributed largely to differences in contact resistance between the nanoprobe and the top of the CNT via among devices. Variations among vias with the same width are mainly due to differences in interface morphology between the nanoprobe and CNT tips, resulting in different numbers of graphene shells making contact with the probe. For via top contact, it is essential that the metal (nanoprobe or contact metal layer) creates a current path through as many CNT walls as possible. We use a nanoprobe with W tip which can be softened by current annealing, effectively increasing the contact area and resulting in carrier flow through the maximum number of CNT walls. Based on such considerations and for the given areal density, we believe that if all process and probing steps are approaching optimum, the via resistance can be as low as 150 Ω for a 60 nm via as measured here. However, variations in contacts (both base and top) among vias, coupled with the fact that a different percentage of CNTs reaching the top of each via, create a substantial scatter in the measured data. Nevertheless, by measuring multiple devices and performing a standard statistical analysis, we can systematically study the downward scaling trend of CNT via resistance, which in turn provides a reasonable projection for future technology nodes.

Since R_m is at least one order of magnitude lower than R_{via}, it is neglected in rewriting Eq. (2) as

$$log(R_{via}) = log[R_{ci}/D_{CNT} + \rho_{CNT} \times h/(D_{CNT} \times A_{CNT})] - 2log(w). \quad (3)$$

Based on Eq. (3) and statistical linear regression analysis of the measured data plotted in a log-log scale, the slope of the fitted line is −1.9, compared to the ideal case of −2 where D_{CNT}, A_{CNT}, and ρ_{CNT} are width-independent, thus supporting this analysis scheme for examining the downward scaling trend of via performance. This result also suggests that the dependence of D_{CNT}, A_{CNT}, and ρ_{CNT} on w may not be significant, which further attests to uniformity in CNT growth. By extrapolating the fitted line, the projected resistance for a 30 nm CNT via with a height of 130 nm is 6.3 kΩ, and can be as low as 295 Ω in the best (or minimum resistance) case.

TABLE I

SUMMARY OF REPORTED CNT VIA RESULTS, CITED IN REVERSE CHRONOLOGICAL ORDER, WHERE W, D, AND H DENOTE VIA WIDTH, DIAMETER, AND HEIGHT, RESPECTIVELY, AND R_{via} THE TOTAL RESISTANCE OF A SINGLE VIA. THE CORRESPONDING EXTRACTED VIA RESISTANCES FOR Cu AND W ARE GIVEN FOR COMPARISON. BOTH BEST-CASE AND AVERAGE RESULTS ARE INCLUDED IN THIS COMPARISON WHEREVER AVAILABLE

	YEAR	GROWTH TEMPERATURE	VIA DIMENSIONS ($W\times H$ OR $D\times H$)	R_{VIA} (BEST)	R_{VIA} (AVER.)
THIS WORK		700 °C	60 nm×130 nm	150 Ω	1.7 kΩ
			30 nm×130 nm	295 Ω	
Cu [16,17]			30 nm×130 nm	24 Ω	
W [17]			30 nm×130 nm	~60 Ω	
[6]	2014	425 °C	100 nm×190 nm	~1.4 kΩ	
[7]	2014	350 °C	1.5 μm×1 μm	~300 Ω	691 Ω
[8]	2013	540 °C	150 nm×300 nm	~400 Ω	2.2 kΩ
[9]	2013	540 °C	150 nm×195 nm		3.4 kΩ
[10]	2012	450 °C	160 nm×100 nm	1.5 kΩ	
[11]	2011	470 °C	300 nm×230nm	4.4 kΩ	
[12]	2011	600 °C	80 nm×250 nm	293 Ω	
[13]	2010	450 °C	160 nm×120 nm	34 Ω	
[14]	2005	700 °C	30 nm× 150nm	7.8 kΩ	

To examine the contributions of the contact resistance R_C and the intrinsic CNT resistance R_{CNT}, we have computed the CNT areal density by directly counting the numbers of CNTs inside a large number of vias of different widths, yielding an average of $\sim 2 \times 10^{11}/\text{cm}^2$. Using $R_{ci} = 300\ \Omega$ [5], R_C is estimated to be 42 Ω for a 60 nm via. By including $R_m = 15\ \Omega$ and the best measured R_{via} value of 150 Ω for a 60 nm via, $R_{CNT} = 93\ \Omega$ for the 60 nm via. Table I lists recently reported experimental results for CNT vias [6]–[14]. Although there are considerable differences among these reports in fabrication processes, measurement techniques, and data analysis methods, our best result of 150 Ω for a 60 nm via represents the lowest reported measured resistance for sub-100 nm CNT vias, albeit at a relatively high CNT growth temperature.

Finally, we examine the potential of CNTs as replacements for current interconnect materials in advanced technology nodes. According to ITRS 2013 [15], metal-1 half-pitch is now entering the 30 nm range and considerable reliability and performance issues with Cu interconnects are expected. Tungsten has also been introduced as the bit-line interconnects material for its advantage in metallization process and electromigration resistance. Based on the experimental work on Cu via [16] and the projected resistivity of 7 μΩ·cm at 30 nm linewidth [17], the resistance of a 30 nm-wide, 130 nm-high Cu via is estimated to be about 24 Ω. For W, with a much higher resistivity of 38 μΩ·cm at 30 nm linewidth [17], the resistance of a 30 nm-wide, 130 nm-high W via is ~60 Ω, including ~5 Ω of contact resistance. These values are included in Table I for comparison with their projected best-case CNT counterpart of 295 Ω. Thus CNT via resistance still needs much improvement to truly competitive, even though CNT seems ideal for high A/R structures and has a significantly higher current density than that of either Cu or W [18]. It is suggested that an areal density of $\sim 1 \times 10^{13}/\text{cm}^2$ for a metallic single-walled CNT ~30 nm-wide via would have comparable resistance to that of Cu, assuming a perfect contact interface [15]. For a via containing multi-walled CNTs with an average of 10 graphene shells per nanotube, a density of $\sim 1 \times 10^{12}/\text{cm}^2$ would provide similar performance. If such packing density can be realized, overcoming high contact resistance will be the remaining hurdle to achieve high-performance CNT vias, with resistances comparable or less than those of their Cu counterparts.

IV. CONCLUSION

From measured resistances of CNT vias with widths 150 nm to 60 nm, we have demonstrated that CNT via performance is beginning to approach those of W and Cu, though more improvements in CNT growth and contact resistance are still needed to be truly competitive. The lowest measured resistance for a 60 nm-wide, 130 nm-high CNT via is 150 Ω, with a statistical average of 1.7 kΩ and standard deviation between 420 Ω and 7.1 kΩ. Statistical analysis has been performed to yield a best projected resistance of 295 Ω for a 30 nm-wide CNT via, five times its W counterpart. Such improvements will eventually enable functionalized CNT via interconnects for next-generation IC technology nodes to be within reach.

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