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## Conductive contact area estimation for carbon nanotube via interconnects using secondary-electron imaging

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A major challenge for carbon nanotube (CNT) to become a viable replacement of copper and tungsten in the next-generation on-chip via interconnects is the high contact resistance between CNT and metal electrodes. A first step in meeting this challenge is an accurate characterization of via contact resistance. In this paper, the scanning electron microscope (SEM) image contrast at low landing energy is employed to estimate the conductive CNT area inside vias. The total conductive CNT area inside each via is deduced using SEM image with 0.1 keV landing energy and a specified threshold brightness, yielding via resistance versus CNT area behavior, which correlates well with electrical nanoprobe measurements of via resistance. Monte Carlo simulation of secondary electron generation lends further support for our analysis and suggests that the residue covering the CNT does not affect the conduction across the contact for residue thickness below 1 nm. This imaging and analysis technique can add much value to CNT via interconnect contact characterization.

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### I. INTRODUCTION

Carbon-based nanostructures such as carbon nanotubes (CNTs), carbon nanofibers (CNFs), and graphene are candidate materials for the next-generation integrated circuit fabrication due to their high current-carrying capacities and excellent electrical, thermal, and mechanical properties.<sup>1–3</sup> The key performance-limiting factor continues to be high contact resistance at the interface with metal electrodes,<sup>4</sup> which inhibits continuous downward device scaling,<sup>5</sup> and is particularly problematic in the nanoscale for device structures consisting of vertical CNTs in contact with a horizontal metal surface.<sup>6,7</sup>

To evaluate the performance of CNTs as on-chip interconnects, it is important to study not only the individual CNTs but also the interconnect devices such as vias.<sup>8,9</sup> We have recently reported results for CNT vias from 60 nm to 150 nm in width, from which the projected 30 nm via resistance approached its tungsten (W) and copper (Cu) counterparts,<sup>10</sup> though substantial improvement of via contact resistance is still needed to make practical use of such devices.

One underlying problem in improving via contact resistance lies in the accurate determination of true contact area between CNTs and the top metal electrode.<sup>11</sup> For macroscale areas, they can be estimated from contact resistance measurements,<sup>12,13</sup> or from direct imaging of the area of a metallic film in contact with an optical microscope through a transparent material.<sup>14–16</sup> For nanostructures such as CNTs, scanning electron microscope (SEM) imaging technique has been used to determine contact areas.<sup>17–19</sup> To extract CNT via contact resistance from resistance measurements, one must know which CNTs inside each via contribute to the

conduction process. To obtain such knowledge, we employ the technique proposed by Suzuki *et al.* using low-voltage scanning electron microscopy (LVSEM) to determine the total conductive CNT area inside each via.<sup>19</sup> For quantitative area analysis, image segmentation analysis from conventional one-level thresholding is also used.<sup>20</sup> The resulting via resistance versus CNT area behavior is analyzed to yield the contact resistance and to correlate with our image analysis. Further, Monte Carlo simulation of the secondary electron (SE) generation provides additional support for our analysis.

### II. EXPERIMENTAL METHODS

The experimental approach is threefold. First, test via devices are prepared using a combination of conventional integrated circuit fabrication and CNT growth processes. Second, SEM images of vias are obtained and the LVSEM technique is employed to determine the exposed CNT areas. Finally, in conjunction with image analysis, *in situ* electrical measurements using a nanoprobe are carried out for the same CNT vias in the SEM image to yield via resistance versus contact area behavior.

#### A. Test structure fabrication

Figure 1(a) presents a cross-section schematic of electrical probing of a CNT via, while Figs. 1(b) and 1(c) show the SEM images of a 500 nm wide via before and after surface polishing, respectively. To fashion this test structure, we start with a 100 mm Si wafer covered by 50 nm of thermal oxide to isolate substrate conduction. The metal underlayer for the vias is formed by a physical vapor deposition of a 20 nm titanium (Ti) layer followed by a 200 nm platinum (Pt) film. A 500 nm low-temperature oxide (LTO) film is then deposited on top of Pt using plasma-enhanced chemical vapor deposition (PECVD) and is patterned using projection lithography

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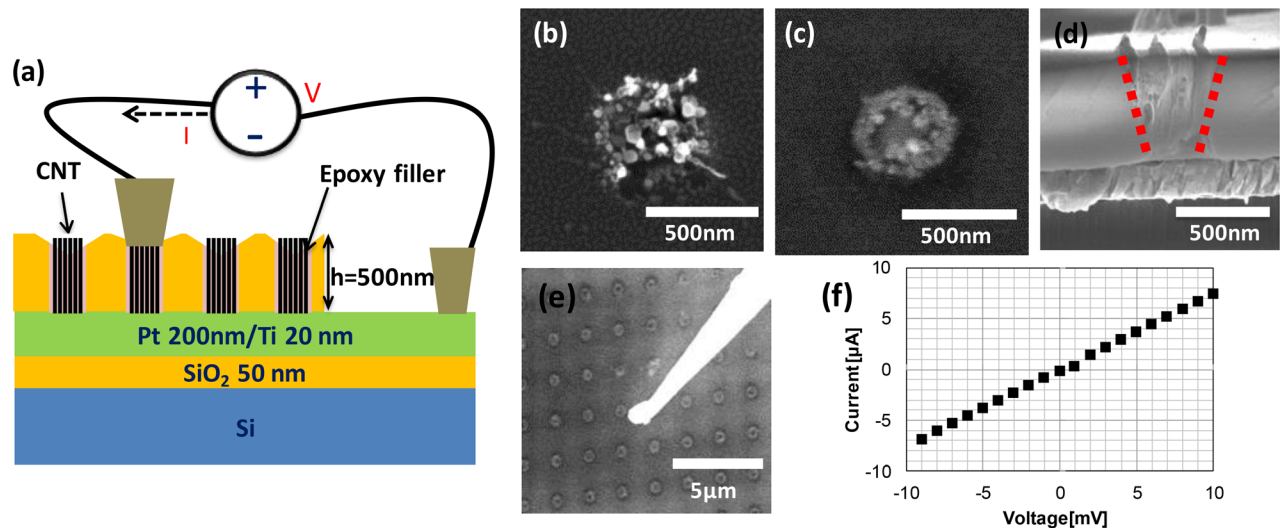


FIG. 1. (a) Cross-sectional schematic of electrical probing of CNT via test structure. (b) Top-view SEM image of a single CNT via before polishing. (c) Top-view SEM image of the same via after polishing. (d) Cross-sectional SEM image of a CNT via. Red dotted lines indicate the via sidewalls. (e) SEM image of a nanoprobe making contact with a via. (f) Typical I-V curve between top of CNT via and Pt/Ti underlayer.

with 5:1 stepping ratio. Vias with a diameter of 500 nm are patterned and formed in the LTO layer using reactive ion etching. After patterning and cleaning, the sample is subjected to electroplating to deposit Ni (used as catalyst for subsequent CNT growth) selectively inside vias, using 0.1 M of nickel sulphamate solution mixed with boric acid diluted in 100 mL of deionized water, at a constant current density of 1 mA/cm<sup>2</sup>, resulting in a 50 nm Ni film formed inside each via. The sample is then baked for 1 h at 250 °C in high vacuum to remove impurities such as sulphur. To grow CNTs inside vias, a PECVD process is employed, in which the sample is initially heated in an ammonia gas ambient at 650 °C to reduce the surface oxide on Ni and to dewet the Ni film. The resulting Ni particles act as sites for CNT growth and the particle size determines the CNT diameter. The temperature is then ramped up to 700 °C and acetylene is introduced in the chamber with an acetylene-ammonia ratio of 1:4, serving as the carbon source, while ammonia acts as a reducing agent to remove the excess amorphous carbon in order to facilitate the CNT growth process. CNTs are grown to about 1 μm in length so as to ensure that all CNTs are taller than the via height. Subsequently, epoxy is deposited on the entire sample as a filler inside vias and to provide a mechanically stable structure for electrical probing. Excess epoxy and the protruding portions of CNTs are removed by mechanical polishing, which also smoothens the surface and exposes the CNT shells for subsequent metallization and electrical probing.

## B. SEM imaging and electrical characterization

Cross-sectional SEM image of a fabricated 500 nm CNT via is shown in Fig. 1(d). Current-voltage (I-V) characteristics of individual CNT vias are measured *in situ* using a pair of tungsten nanoprobes inside a SEM chamber, as shown schematically in Fig. 1(a),<sup>7</sup> and an image of a nanoprobe landing on a via is captured in Fig. 1(e). We employ the current stressing technique to reduce the contact resistance and achieve stability of the I-V results.<sup>7</sup> Reproducibility of the

resistance is estimated to be about ±20%. The results are not sensitive to the accuracy of the probe position resting on top of the CNT via. This is attributed to the size of the probe tip being larger than the diameter of CNT via. The probe placement is controlled by a piezoelectric drive, and pressure is applied until the measured I-V characteristic does not change by a minimal increment of the probe pressure. A typical I-V curve after current stressing between the top of a CNT via and the Pt/Ti underlayer is shown in Fig. 1(f).

Elemental maps obtained from energy-dispersive x-ray spectroscopic (EDS) analysis of a CNT via using an accelerating voltage of 10 kV are shown in Fig. 2. Silicon (Si) and Oxygen (O) from SiO<sub>2</sub> are detected around the via, while a large amount of carbon (C) from CNTs is detected inside the via perimeter. Comparing the elemental map of C with the bright contrast of the secondary electron (SE) image, a strong correlation is found due to the edge contrast resulting from the difference in conduction through a CNT and the surrounding epoxy by an electron-beam-induced current,<sup>21</sup> which is elaborated in Sec. III. Also a large amount of Pt from the underlayer is detected inside the via, due mainly to the difference in primary electron (PE) stopping power between C (from CNT and epoxy) and Si from the LTO surrounding the via.

To identify the exposed CNTs inside each via, which can make electrical contact with the nanoprobe, SE LVSEM imaging is employed in a field-emission scanning electron microscope (Hitachi S-4800), at electron landing energies of 0.1 keV, 0.3 keV, and 0.5 keV. The SEM is equipped with an in-column SE detector for low-energy (less than several tens of eV) electron detection. In order to analyze SEM images quantitatively, we adjust the image brightness offset to zero when no signal is detected.

To determine the total conductive CNT area and to differentiate the images from the three accelerating voltages, we need to minimize the effect of the PE beam spot size and the differences in current from different PE energies. To achieve this, we set the working distance at 1.5 mm and the

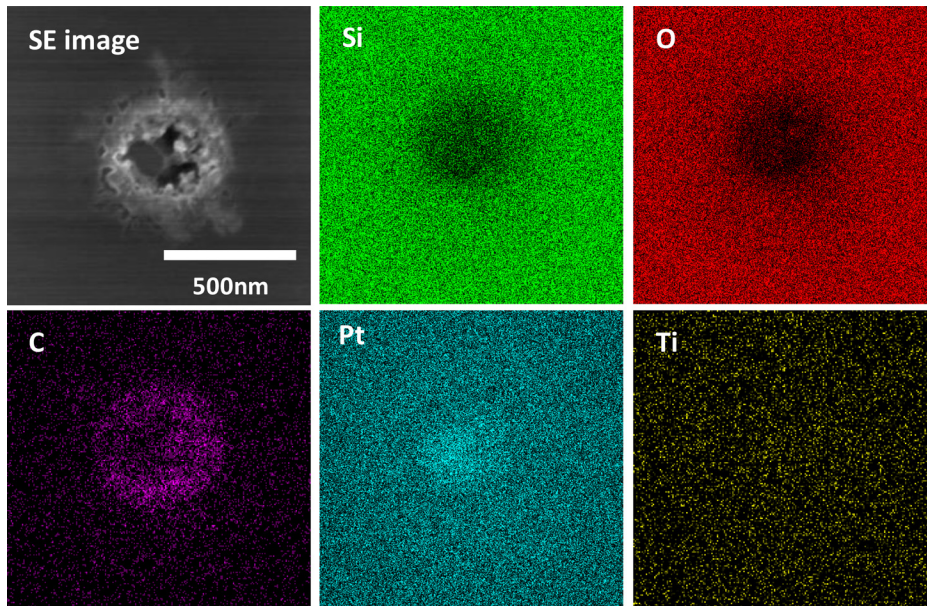


FIG. 2. Top-view SEM image of CNT via and EDS elemental maps for Si, O, C, Pt, and Ti using an accelerating voltage of 10 kV. Large amount of C is present inside the via as expected, and significant amount of Pt from the underlayer is detected inside the via as well.

displayed working distance at 0.9 mm to get a small PE beam spot size. And we select a SEM image pixel size of 4.1 nm, much larger than the beam spot size for each landing energy. Further, to obtain the same PE beam current and same sample charging effect throughout our experiments, we use the same 0.6 kV accelerating voltage for imaging and adjust the landing energy using sample bias (SEM deceleration mode). Thus, the sample biasing voltages of 0.5 kV, 0.3 kV, and 0.1 kV result in electron landing energies of 0.1 keV, 0.3 keV, and 0.5 keV, respectively. The sample bias is applied to the Si substrate. In order to locate the CNT via under test easily, the pixel resolution is set to  $5120 \times 3840$  with an image field of view of  $21.0 \mu\text{m} \times 15.7 \mu\text{m}$ , and we crop each CNT via image after obtaining a larger one.

### III. RESULTS OF IMAGE ANALYSIS

The procedure to obtain the conductive CNT area inside a via is illustrated in Fig. 3. It was suggested that single-

walled CNTs produce bright contrast of the insulator surface at low PE accelerating voltage,<sup>21</sup> since the insulator region surrounding the CNT emits more secondary electrons due to electron-beam-induced current. Based on such findings, we proceed to estimate the exposed CNT area from each via LVSEM image using a conventional threshold method that determines the area brighter than the threshold.

Because of the difference in SE yield among different PE beam energies, we normalize the image brightness using the brightest pixel (maximum brightness) for each primary beam energy, or normalized brightness  $t_{TH} = \text{threshold brightness}/\text{maximum brightness}$ . To reduce the normalization error, a large field of view,  $21.1 \mu\text{m} \times 15.9 \mu\text{m}$ , is used, which contains the 96-via LVSEM image shown in Fig. 3(a). The maximum pixel brightness is determined by using the image histogram in Fig. 3(b). Further, each CNT via image is obtained by cropping the large field of view image to minimize the brightness error arising from capturing the image multiple times, resulting in the image shown in Fig. 3(c).

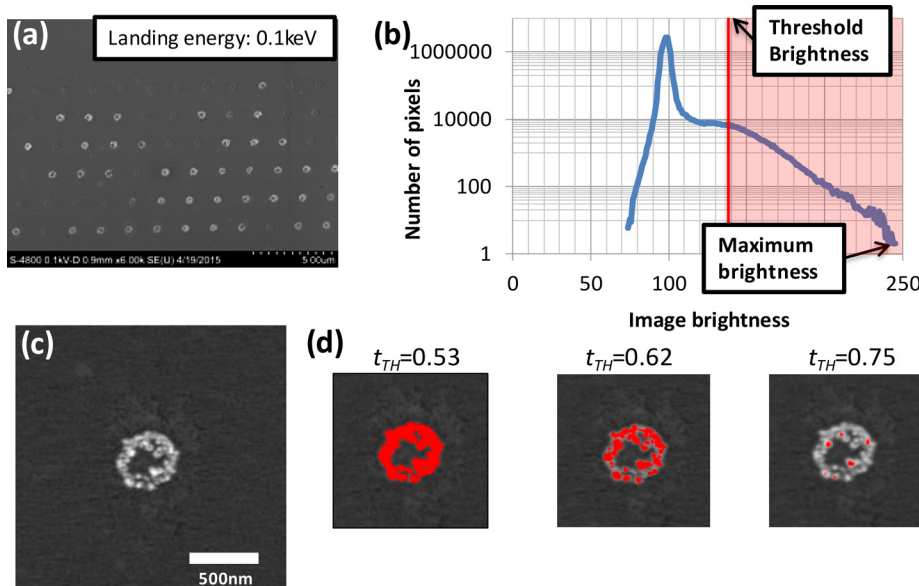


FIG. 3. Image analysis summary. (a) LVSEM image of a  $12 \times 8$  array of CNT vias. (b) Histogram of the LVSEM imaging to determine maximum and threshold brightness. (c) LVSEM image of a CNT via from (a). (d) Brightness contrast area map of CNT vias for  $t_{TH} = 0.53, 0.62,$  and  $0.75$ , where  $t_{TH}$  is threshold brightness divided by maximum brightness for each SEM image. Red pixel indicates brightness above threshold, corresponding to exposed CNT areas with brightness above threshold. Delete redundant definition of  $t_{TH}$  in figure.

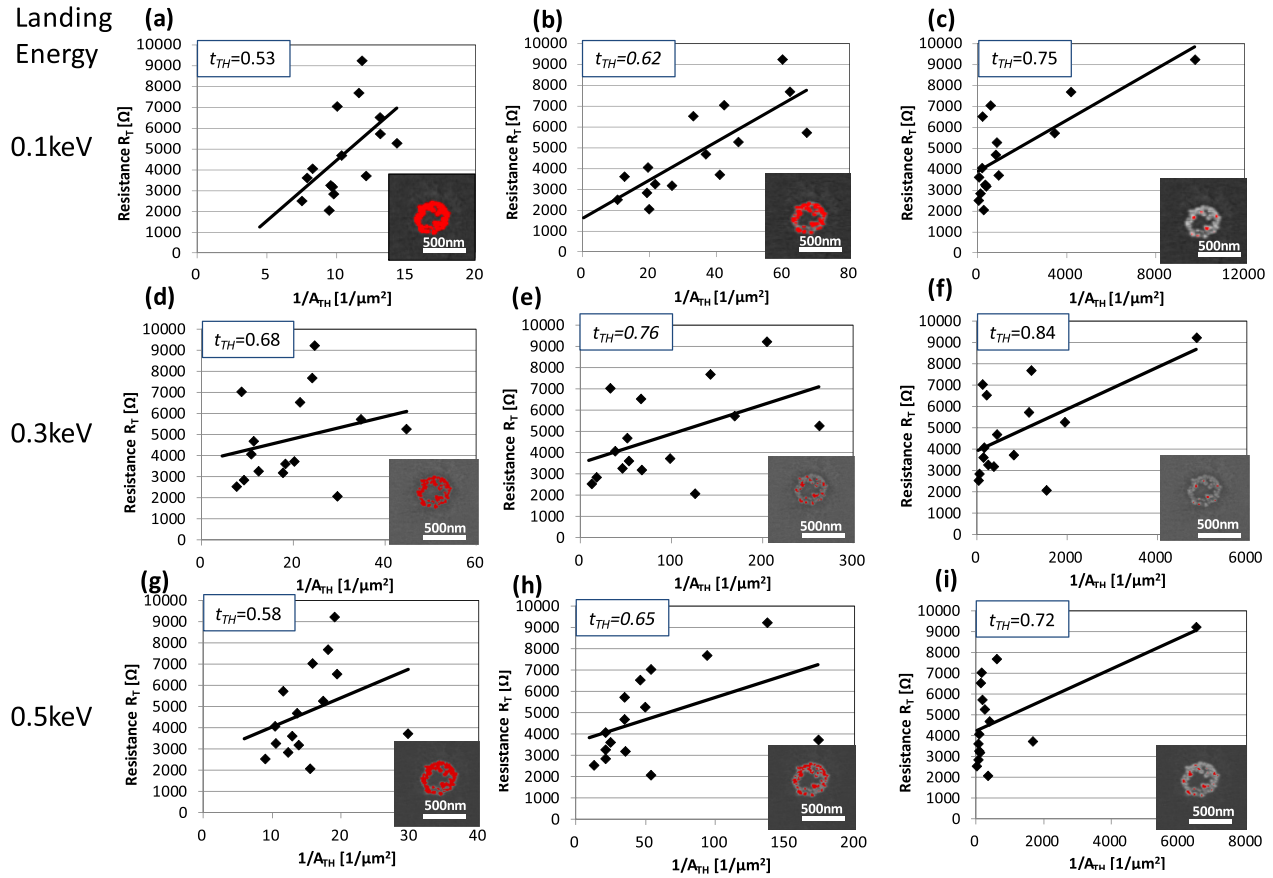


FIG. 4. Measured via resistance  $R_T$  versus  $1/A_{TH}$  plots for 15 vias, at 0.1 keV [(a)–(c)], 0.3 keV [(d)–(f)], and 0.5 keV [(g) and (h)], and various  $t_{TH}$ . Each linear fit is based on Eq. (1). LVSEM image of one of the vias is shown in the inset for each plot.

use Fig. 3(b) to define a threshold brightness in the LVSEM image and determine the total area brighter than the threshold, as illustrated in Fig. 3(d). The threshold brightness corresponding to the exposed CNT area changes with image acquisition condition and image sharpness, as well as pixel size and PE landing energy. Thus, a number of exposed CNT areas  $A_{TH}$  are obtained using several brightness thresholds

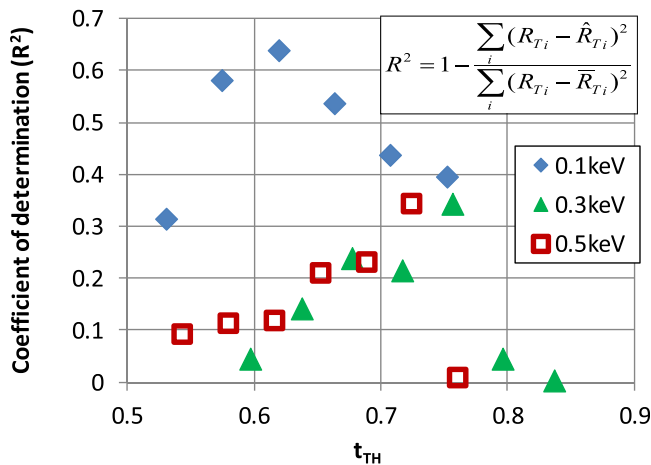


FIG. 5. Coefficient of determination  $R^2$  versus  $t_{TH}$  for linear fits of  $R_T$  versus  $1/A_{TH}$  data at 0.1 keV, 0.3 keV, and 0.5 keV landing energies.  $R^2$  formula is given in inset with each term defined in the text. The value of  $A_{TH}$  corresponding to the highest  $R^2$ , occurring at 0.1 keV and  $t_{TH}=0.62$ , is defined as  $A_{BEST}$ .

for each landing energy to yield the best fit to the via resistance  $R_T$  versus  $1/A_{TH}$  behavior, resulting in  $A_{BEST}$ , as described below.

$R_T$  obtained from the measured I-V curves consists of contributions from CNTs ( $R_{CNT}$ ), CNT/metal underlayer and CNT/probe contacts ( $R_C$ ), metal underlayer, probes, and probe/metal contact. The latter three are via-independent and can be lumped together as  $R_m$ . Thus,  $R_T = R_m + R_C + R_{CNT}$ .<sup>10,22</sup> Assuming that the ohmic conduction and all the

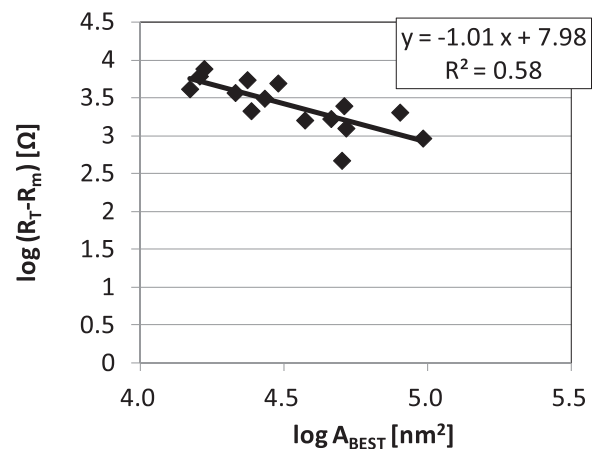


FIG. 6. Log-log plot of  $(R_T - R_m)$  versus  $A_{BEST}$  based on assumptions underlying Eq. (1). Slope of the linear fit is  $-1.01$ , compared to the ideal case of  $-1$ .

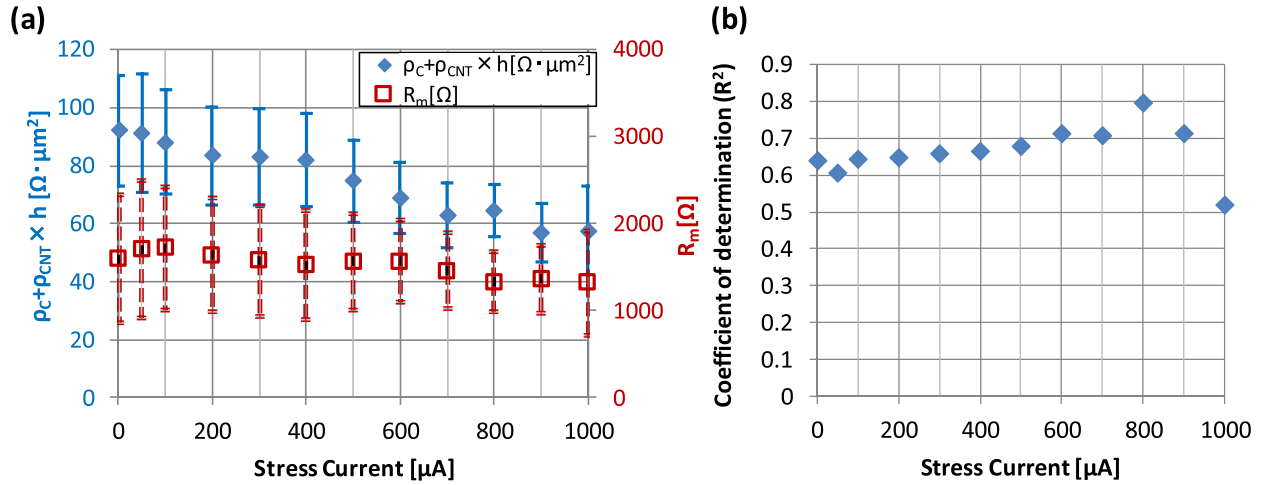


FIG. 7. (a) Behaviors of  $(\rho_C + \rho_{CNT} \times h)$  and  $R_m$  components of via resistance upon current stressing for the same 15 vias used for Figs. 4–6, as extracted from  $R_T$  versus  $I/A_{BEST}$  plots. The average and range of each extracted component are indicated as points and error bars, respectively, for each stress current. (b)  $R^2$  for linear fit of  $R_T$  versus  $I/A_{BEST}$  peaks at stress current of 800  $\mu\text{A}$ .

exposed CNTs possess the same resistivity  $\rho_{CNT}$  and length  $h$ , which is the via height for a polished sample,  $R_T$  can be rewritten as

$$R_T = R_m + \frac{1}{A}(\rho_C + \rho_{CNT} \times h), \quad (1)$$

where  $\rho_C$  is the contact resistivity and  $A$  the total conductive CNT area inside the via.

To obtain  $A_{BEST}$ , the coefficient of determination ( $R^2$ ) is used to evaluate the linear fit of the  $R_T$  versus  $I/A_{TH}$  plot, based on Eq. (1) and assuming  $(\rho_C + \rho_{CNT} \times h)$  is via-independent. In this case,  $R^2$  is given by Kvalseth<sup>23</sup> as

$$R^2 = 1 - \frac{\sum_i (R_{Ti} - \hat{R}_{Ti})^2}{\sum_i (R_{Ti} - \bar{R}_{Ti})^2}, \quad (2)$$

where for each via  $\hat{R}_T$  is the predicted  $R_T$  value from the linear fit shown in Fig. 4, and  $\bar{R}_T$  is the mean of all  $R_T$  values. Figure 4 shows nine  $R_T$  versus  $I/A_{TH}$  plots for 15 vias, corresponding to nine  $t_{TH}$  values obtained at landing energy of 0.1 keV, 0.3 keV, and 0.5 keV. The LVSEM image of one of the vias is also shown for each of the  $t_{TH}$  values to illustrate the difference among the nine plots. A plot of  $R^2$  versus  $t_{TH}$  for each landing energy is given in Fig. 5. Since the maximum  $R^2$  value is 1, the  $R_T$  versus  $I/A_{TH}$  plot with the largest  $R^2$  indicates the best match, and the corresponding  $A_{TH}$  is  $A_{BEST}$ , obtained at 0.1 keV and  $t_{TH} = 0.62$ . As a result, a relatively large extracted  $R_m$  of 1.6 k $\Omega$  is obtained from the linear fit to the  $R_T$  versus  $I/A_{BEST}$  plot. This large resistance is attributed to the probe-underlayer metal resistance, as the exposed metal surface is most likely oxidized, and to the work function difference between the W probe and the Pt underlayer.<sup>24</sup>

Figure 6 shows a statistical linear regression analysis of  $(R_T - R_m)$  versus  $A_{BEST}$  behavior plotted in the log-log scale. The slope of the linear fit is  $-1.01$ , compared to the ideal case of  $-1$  from taking the logarithm of  $(R_T - R_m)$  in Eq. (1). This analysis provides an independent support of the LVSEM image

analysis. From the intercept of the log-log plot in Fig. 6, the contact resistivity can be deduced with an assumed CNT resistivity value. If we adopt the value of 4 m $\Omega$ -cm, obtained from our previous study<sup>25</sup> on CNTs (referred to as carbon nanofibers then) grown using the same process and instrument as in this study, for the conductive CNTs inside the vias under test, the contact resistance is estimated to be 0.8  $\mu\Omega$ -cm<sup>2</sup>. Thus, the ratio of contact resistance to total conductive CNT resistance inside the via is  $\rho_C/(\rho_{CNT} \cdot h) = 4$  for a 500 nm tall via, consistent with our previous findings.<sup>22</sup> It should be noted, however, that this fraction can be altered by using a different CNT resistivity value. Since the assumed resistivity falls within the range of reported values,<sup>7</sup> and is from CNTs grown with the same process, its use to estimate the via contact resistivity is justified.

#### IV. DISCUSSION

Current stressing experiments are also performed to lend further support for our image analysis. Figure 7(a) shows the behaviors of the extracted  $R_m$  and  $(\rho_C + \rho_{CNT} \times h)$  components of via resistance [Eq. (1)] with increasing stress current for the same 15 vias.  $R_m$  is virtually unchanged as expected, as it is via-independent, while a significant drop in  $(\rho_C + \rho_{CNT} \times h)$  occurs with an increase in stress current, due largely to a decrease in contact resistance, and completely consistent with the previously reported reduction of CNT-metal contact resistance by current stressing.<sup>25–28</sup> The corresponding  $R^2$  values for fitting  $R_T$  versus  $I/A_{BEST}$  data are given in Fig. 7(b) as a function of stress current. The  $R^2$  value lingers around 0.65 until it peaks at 0.8 at a stress current of 800  $\mu\text{A}$  before dropping to  $\sim 0.5$  at 1000  $\mu\text{A}$ , suggesting that the contact interface may have been changed by Joule heating at currents  $\sim 800$   $\mu\text{A}$  and higher.<sup>26,27</sup>

To examine the SEM-derived CNT conductive area inside a via, we describe the SEM image formation mechanism using a schematic diagram shown in Fig. 8. If a CNT is unexposed due to coverage by residue (case (a) in Fig. 8), it would show no contrast with the epoxy using very low-energy PE beam, as the PE beam cannot penetrate the residue to reach the CNT, thus positively charging the residue and forming a potential barrier to block emitting SEs.<sup>19</sup> In

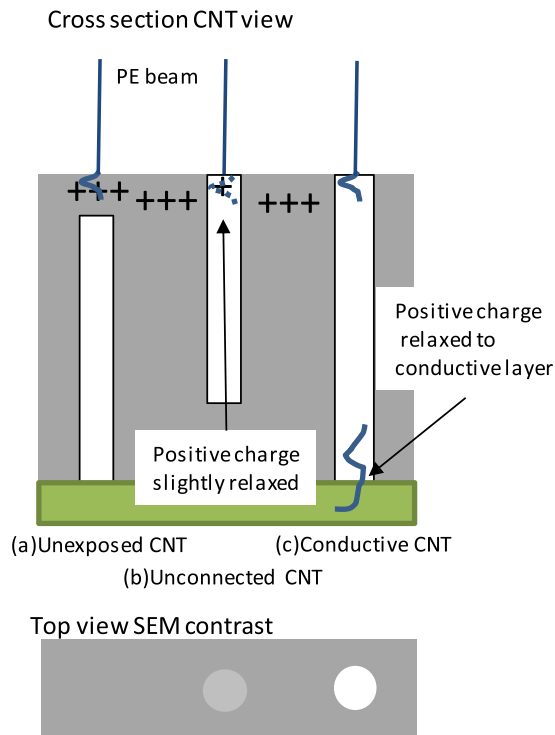


FIG. 8. Schematic of SEM image formation mechanisms for (a) unexposed CNT (non-conductive), (b) unconnected CNT (non-conductive), and (c) CNT connected to conductive layer.

the case of an unconnected CNT [case (b)], the positive charge is slightly relaxed due to an electron-beam-induced current.<sup>21</sup> As a result, the contrast is low. When the CNT is connected to a conductive layer [case (c)], the positive

charge is fully relaxed, revealing a distinguishable contrast. These image formation mechanisms make it possible to distinguish between conductive and non-conductive CNTs using LVSEM imaging and conventional threshold methods, and to determine the conductive area reliably.

To study these observed phenomena quantitatively, we simulate the SE generation using the Monte Carlo method. In our previous studies,<sup>29,30</sup> we have developed Monte Carlo simulation codes to simulate the scattering process of PEs in the carbon specimen and the generation of SEs. In the codes, Mott cross-sections are implemented for elastic scattering and a continuously slowing-down approximation is assumed for averaged inelastic processes.<sup>29</sup> For SE emission, the mean free path of 5.5 nm and the mean generation energy of 125 eV are used to reproduce the experimental SE yield of carbon (mass density of 2.26 g/cm<sup>3</sup> is assumed).<sup>31</sup> Figure 9(a) shows the simulated PE spread with 100 trajectories inside a carbon sample at landing energies of 0.1 keV, 0.3 keV, and 0.5 keV, respectively. The LVSEM image of a CNT via for each landing energy is also shown for comparison. The 0.5 keV image is more blurred compared to the 0.1 keV one, due to the larger spread of PE at 0.5 keV. The 0.3 keV image has shades around the via edge and the contrast between the epoxy and CNT is less, mainly due to a high SE yield of the dielectric material<sup>32,33</sup> and a deeper SE generation depth at 0.3 keV. Figures 9(b) and 9(c) show the lateral (x direction) and depth (z direction) distributions of the secondary electron generation points simulated under 10 000 PEs, respectively, for the three landing energies. The blurred image at 0.5 keV is consistent with the horizontal spread of the SE generation as evident in Fig. 9(b), with the

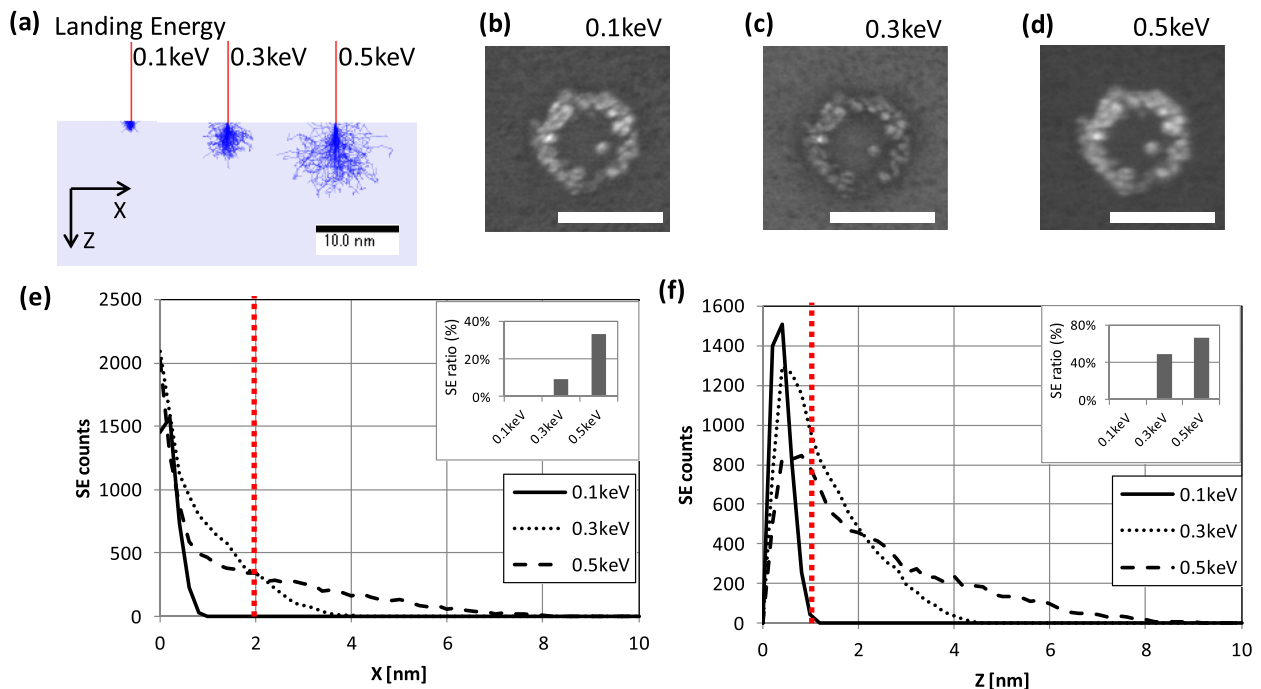


FIG. 9. Monte Carlo simulations of SE generation in a carbon sample. (a) 100 PE trajectories at landing energies of 0.1 keV, 0.3 keV, and 0.5 keV. PE beam is indicated in red impinging perpendicularly upon the carbon sample and scattered electrons inside the sample in blue. [(b)–(d)] Top-view SEM images of via for landing energies of 0.1 keV, 0.3 keV, and 0.5 keV, respectively, with each scale bar being 500 nm. (e) Lateral distribution of SE generation site under 10 000 PE inputs. Inset indicates SE ratio (in %) defined as the number of SEs generated farther than 2 nm from center divided by the total number of generated SEs. (f) Depth distribution of SE generation site. Inset shows SE ratio, defined as the number of SEs generated deeper than 1 nm divided by total number of generated SEs.

inset showing the SE ratio generated beyond 2 nm. In the case of 0.5 keV, 33% of SEs are generated beyond 2 nm, which is larger than the image pixel size, accounting for the blur. On the other hand, for 0.1 keV, all SEs are generated within 2 nm. The blurred image at 0.5 keV precludes an accurate determination of the CNT area based on our analysis.

The difference between the 0.1 keV and 0.3 keV images is attributed to the difference in SE generation depth since it is less with lower landing energy, as shown in Fig. 9(c). Suzuki *et al.* suggested that a thin residue layer might be present on some CNTs, which inhibits conduction through the CNT, and a low-energy PE is required to distinguish between covered and uncovered CNTs.<sup>19</sup> Assuming that the residue is amorphous carbon, the simulated SE generation depth shown in Fig. 9(c) and the LVSEM images in Fig. 9(a) suggest that at 0.1 keV, the residue on CNT does not affect the CNT electrical contact if less than 1 nm thick. This finding is consistent with the dependence of tunneling current on the thickness of an interfacial layer across a CNT-metal contact.<sup>27</sup> Thus, the simulation results support our choice of using 0.1 keV landing energy images to determine the conductive CNT area inside each via.

## V. CONCLUSIONS

In summary, we have successfully determined the total conductive CNT area inside each via interconnect test device using the LVSEM technique. Our results correlate well with measured resistance versus CNT area behavior. Current stressing experiments are performed on the vias to validate the image analysis and to elucidate the role of contacts in the via structure. Monte Carlo simulation of SE generation lends further support for our image analysis and suggests that the residue covering the CNT does not affect the conduction across the contact for residue thickness below 1 nm. The image analysis technique can be used for the characterization of CNT via interconnects.

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<sup>1</sup>See <http://www.itrs2.net/2013-itrs.html> for International Technology Roadmap for Semiconductors (ITRS), Metrology (The Semiconductor Industry Association, 2013).

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