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Breakdown voltage of ultrathin dielectric film subject to electrostatic discharge stress

Hao Jin,[1] Shurong Dong,[1,a)] Meng Miao,[1] Juin Jei Liou,[1,2] and Cary Y. Yang[1,3]
[1]*Department of ISEE, Zhejiang University, Hangzhou, 310027 People's Republic of China*
[2]*Department of EECS, University of Central Florida, Orlando, Florida 32816, USA*
[3]*Center for Nanostructures, Santa Clara University, Santa Clara, California 95053, USA*

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Ultrathin silicon oxide film for nano-electromechanical system (NEMS) applications is investigated under electrostatic discharge (ESD) stress using a transmission line pulse (TLP) tester. The measured breakdown voltage and transient response are analyzed. The results show that the voltage stress time has a significant effect on the breakdown voltage. By shortening the stress time, the breakdown voltage increases by 2–3 times. With the area shrinking breakdown voltage increases, and there is a critical value, below which the breakdown voltage increases dramatically with decreasing area. It is possible to enhance the ESD robustness by using a multiple small-area dielectric layer structure. Shorten ESD pulse rise-time induces a higher overshoot current and then accelerates oxide failure, resulting in a lower breakdown voltage for a faster pulse. © *2011 American Institute of Physics*. [doi:10.1063/1.3633527]

I. INTRODUCTION

Ultrathin silicon oxide films are widely used in nanodevices to provide electrical insulation, mechanical support, and/or masking, such as nano-electromechanical system (NEMS) and advanced complementary metal-oxide-semiconductor (CMOS) devices. Electrostatic discharge (ESD) is a prevailing challenge for the reliability of silicon[1–3] or non-silicon nanodevices,[4–6] as the dielectric layers embedded in these devices can easily break down when subjected to an ESD stress. Ultrathin dielectric film in nanodevices makes the ESD-induced breakdown even more prominent.[7] It is therefore imperative to understand the behavior of ultrathin dielectric films under ESD stress in designing robust nanodevices. Previous studies on ultrathin dielectric film breakdown under ESD stress were carried out using various test structures related to the intended applications.[2,4] In CMOS devices, ESD breakdown of gate oxide was investigated using a MOS test structure, and its breakdown behavior was shown to depend on the substrate type (p or n) and V_g.[2,3] ESD breakdown of dielectric film employed in NEMS was evaluated using a film with air gap in RF-MEMS capacitive switches.[4,5]

To focus on the behavior of an ultrathin oxide film under ESD stress in order to assess its robustness, it should be examined without the use of a complex test structure, to avoid the influence of additional variables. In this paper, we report the breakdown characteristics of silicon oxide layers subject to various ESD stresses using a transmission line pulse (TLP) tester. The results yield an enhanced understanding of the breakdown mechanisms in ultrathin oxide films.

II. EXPERIMENTAL DETAILS

Test devices (DUTs) containing ultrathin silicon oxide layers have been fabricated at the Semiconductor Manufacturing International Corporation (SMIC) and their schematic is shown in Fig. 1(a). The oxide layers were deposited on a silicon wafer using plasma-enhanced chemical vapor deposition (PEVCD). The electrodes were made of polysilicon and insulated with the shallow trench isolation (STI) technique.[14] The depth of STI is 150 nm, the depth of n^+-well region is 650 nm, and each oxide layer is 1 μm wide. The DUTs, with various areas, thicknesses, and anode-to-cathode distances (OD), were examined using the TLP tester for various ESD pulse-widths and rise times. Note that the anode is placed on the oxide layer and the cathode is on the n^+-well (see Fig. 1(a)) to reduce contact resistance.

After applying each pulse, the leakage current was measured. The oxide layer failure (or breakdown) is defined at the voltage where the leakage current increases from its initial value by two orders of magnitude. The simulated electric field distribution in the DUT is also shown in Fig. 1(a), and a DUT with a damaged silicon oxide layer is shown in Fig. 1(b). The time-dependent dielectric breakdown (TDDB) of the same DUTs was also investigated for comparison.

III. RESULTS AND DISCUSSION

At first, we investigate oxide breakdown behavior with various thickness and voltage over-stress time. As shown in Fig. 2, the voltage stress time have a significant effect on the breakdown voltage. By shortening the stress time, the breakdown voltage increases by 2–3 times. The behavior of breakdown voltage (v) with varying thickness (T) is similar for different voltage stress times, which is not in agreement with the empirical relation $T_1/T_0 = (v_0/v_1)^n$ (Refs. 2 and 13) and the 1/E model.[3,12] This discrepancy is attributed to the fact

a)Electronic mail: dongshurong@zju.edu.cn.

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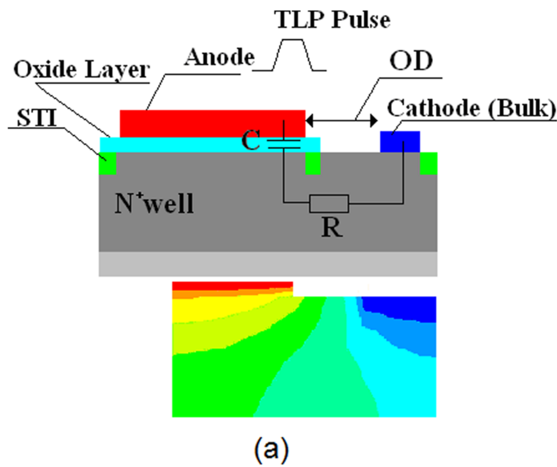

(b)

FIG. 1. (Color online) (a) Cross-section of a test device and electric field obtained from TCAD simulation. (b) Corresponding SEM image showing the damaged oxide layer.

that a longer voltage stress cycle generates more defects in the oxide layer and also provides more energy to create the defect link for oxide to punch through. This behavior is similar to the time-dependent dielectric breakdown (TDDB) mechanism associated with the constant voltage stress (CVS) method.[8]

The oxide thickness also plays an important role in determining the ESD breakdown voltage, as shown in Fig. 2. With the oxide thinning from 5 nm to 1.5 nm, the breakdown voltage decreases, though not linearly, significantly different from the breakdown voltages of these samples under dc stress.[2,3] When the oxide thickness falls below 3 nm, the decrease in breakdown voltage becomes smaller. In general, thinner oxide is more robust under ESD pulse stress than under dc stress. Further, as evident in Fig. 2, the decrease in breakdown voltage with decreasing thickness is much less for thinner oxides.

Since the thicker oxide layer has a higher breakdown voltage than the thinner one, enhanced ESD robustness can be achieved by using a thicker oxide layer. However, it should be kept in mind that an increase in breakdown voltage is not directly proportional to an increase in oxide thickness, and thus cannot be scaled accordingly. The ESD pulse rise time of 10 ns and width of 100 ns are equivalent to those in the human body model (HBM), and the ESD pulse rise time

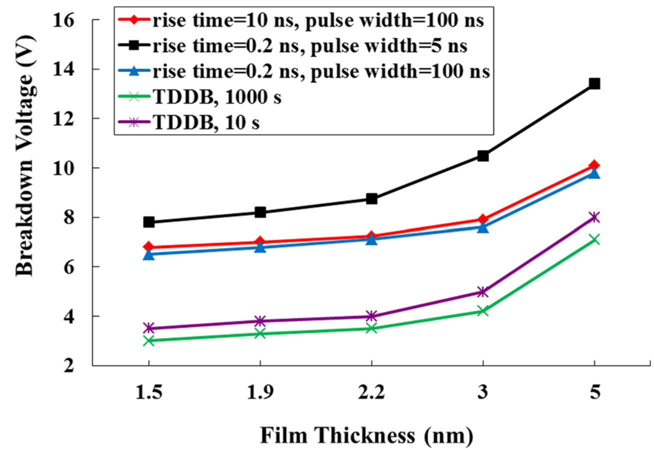

FIG. 2. (Color online) Oxide breakdown voltage vs oxide thickness, OD = 4.05 nm, Area = 1×3 μm^2.

of 0.2 ns and width of 5 ns are similar to those associated with a different ESD event described by the charged device model (CDM). For example, for the 65 nm CMOS process, the oxide layer thickness is 2.2 nm in core NMOS, 3 nm in 1.8 V NMOS and 5 nm in 2.5 V NMOS. The corresponding HBM and CDM breakdown voltages are estimated to be 6–7 V, 7–8 V, 9–10 V, and 8–9 V, 10–11 V, and 12–13 V, respectively.

Figure 3 shows the effect of the increasing oxide film area on the breakdown voltage. There is a critical value, below which the breakdown voltage increases dramatically with decreasing area, and above which the breakdown voltage varies little with area. And this critical value decreases with decreasing oxide thickness. In particular, for oxide thicknesses of 5 nm, 3 nm, and 2.2 nm, the critical areas are 3.5 μm^2, 2.6 μm^2, and 1 μm^2, respectively.

Thus, in designing nanoscale devices, the layout of an ultrathin dielectric layer should be carefully considered, especially when its thickness is below 3 nm. In the case of a 1 μm^2 and 2.2 nm oxide layer, the breakdown voltage is 7.3 V. However, its breakdown voltage can be increased up to 9 V if the oxide layer is divided into two parts with an area of

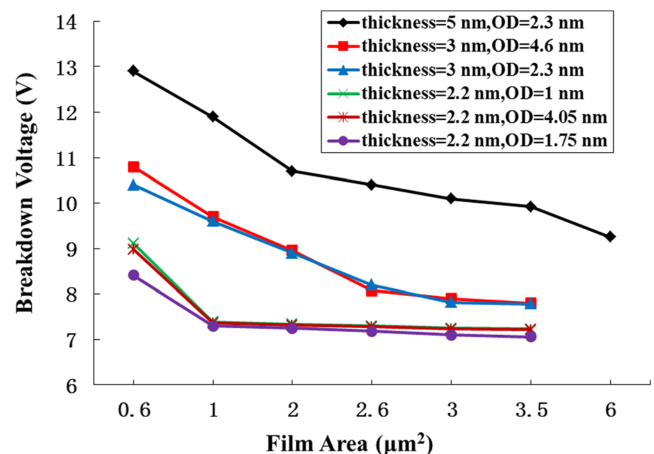

FIG. 3. (Color online) Breakdown voltage vs oxide film area for several oxide films (with thicknesses 2.2, 3, and 5 nm) subject to stress by TLP pulses with pulse width 100 ns and rise time 10 ns, for test devices with various anode-to-cathode distances OD.

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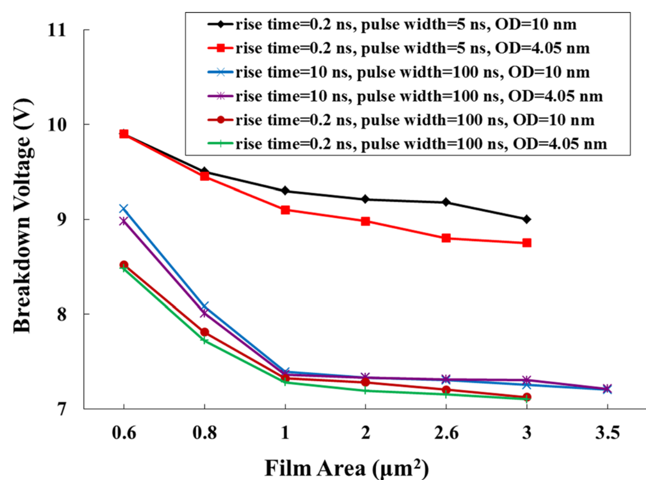

FIG. 4. (Color online) Breakdown voltage for oxide films with thickness = 2.2 nm stressed by TLP pulses with various rise times and pulse widths.

0.5 μm^2 each. This implies it is possible to enhance the ESD robustness by using a multiple small-area dielectric layer structure such as a waffle-like configuration, and the area of each part should be smaller as the oxide becomes thinner.

It is generally known that the defects are responsible for oxide breakdown, and various mechanisms including impact ionization, hole injection, thermochemistry, and hydrogen release under static stress have been introduced to explain defect generation.[9] In addition, the percolation model was used to explain the oxide breakdown behavior.[8,10] According to this model, defects can be generated and distributed randomly inside the oxide. The oxide layer is punched through by the ESD stress only when these defects are linked together to form a discharge route. The larger oxide area gives rise to a higher probability to form such a discharge route, which in turn results in a lower breakdown voltage. Furthermore, as a thinner oxide has a shorter vertical distance and more defects per unit area,[8,9] the defects are more likely to link together than the thicker counterpart under the same oxide area. Thus, a thicker oxide has a lower breakdown voltage than a thinner one with the same area.

The anode-to-cathode distance is an important parameter in designing robust ESD nano-CMOS devices, as it is related to the resistance R shown in Fig. 1(a) and affects the trigger voltage of the grounded-gate n-channel metal–oxide–semiconductor field-effect transistor (GGNMOS).[11] However, our results show that OD has little effect on the breakdown voltage of the devices, as shown in Fig. 3. This can be explained using the TCAD simulated results given in Fig. 1(a), which show that most of the voltage drop is across the oxide layer in the vertical direction rather than in the lateral direction, i.e., along OD. As a result, we can increase the nanodevice areal density by reducing OD without sacrificing EDS robustness.

The ESD robustness of an oxide layer is also related to the characteristics of the TLP pulse. TLP pulses having different rise times (0.2 ns and 10 ns) and widths (5 ns and 100 ns) were applied to several test devices with a 2.2 nm thick oxide. As shown in Fig. 4, pulse width has the dominant effect on the breakdown voltage, yielding lower breakdown voltage for larger pulse width.

Measured TLP transient current waveforms are shown in Fig. 5. The 0.2 ns-rise-time ESD pulse induces a higher overshoot current than that from a 10 ns-rise-time pulse. This overshoot current, which can be considered as the displacement current passing through the oxide capacitor, C, (see Fig. 1(a)), causes a rapid charge accumulation that results in a very large instantaneous voltage v change through the relationship, $I = C \times (dv/dt)$.[7] Consequently the overshoot current accelerates oxide failure, resulting in a lower breakdown voltage for a faster pulse.

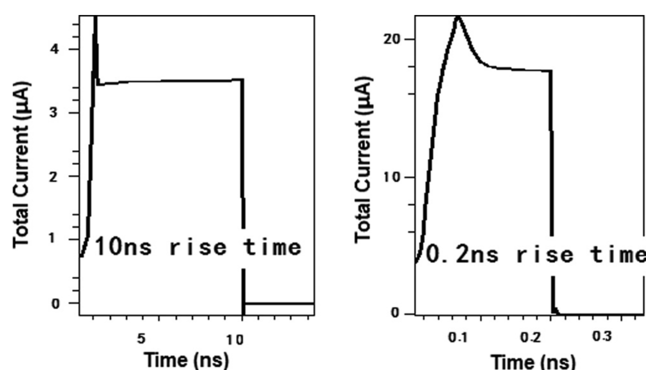

FIG. 5. Transient current behaviors of test devices stressed by two TLP pulses with different rise times, respectively.

IV. CONCLUSIONS

Using the transmission line pulse (TLP) tester, ultrathin oxide films in nanoscale devices subject to electrostatic discharge (ESD) stress reveal a breakdown behavior different from that found for conventional dc stress. The oxide breakdown voltage decreases with increasing oxide area regardless of TLP pulse rise time. Oxide thickness and TLP pulse width also play important roles in the breakdown behavior. This study provides useful information for designing reliable NEMS against various ESD events.

ACKNOWLEDGMENTS

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