



Review paper

Electrical properties of carbon nanotube via interconnects for 30 nm linewidth and beyond



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ABSTRACT

The continuous downward scaling in integrated circuit (IC) technologies has led to rapid shrinking of transistor and interconnect feature sizes. While scaling benefits transistors by increasing the switching speed and reducing the power consumption, it has an adverse impact on interconnects by degrading its electrical performance and reliability. Scaling causes reduction in interconnect linewidth, which leads to surge in resistance due to increased contributions from grain boundary and surface scattering of electrons in the metal lines. Further, current density inside interconnects is also enhanced by the reduced linewidth and is approaching or exceeding the current-carrying capacity of the existing interconnect metals, copper (Cu) and tungsten (W). The resulting failure due to electromigration presents a critical challenge for end-of-roadmap IC technology nodes. Therefore, alternative materials such as nanocarbons and silicides are being investigated as potential replacements for Cu and W as they have superior electrical and mechanical properties in the nanoscale. In this review, the electrical properties of nanocarbons, in particular carbon nanotubes (CNTs), are examined and their performance and reliability in the sub-100 nm regime are assessed. Further, the measured properties are used to project 30 nm CNT via properties, which are compared with those of Cu and W.

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1. Introduction

The aggressive downward scaling in IC technologies following Moore's law has led to shrinking of on-chip feature sizes down to the sub-30 nm regime [1,2]. For interconnects, such shrinking results in

adverse effects on their performance and reliability, due to increases in resistance and current density, respectively, for existing interconnect materials, Cu and W [2]. Increase in resistance is caused by enhanced electron scattering at grain boundaries and surfaces [3–7], leading to increase in propagation delay through interconnect that degrades the circuit performance. The surge in current density approaches or exceeds the current-carrying capacity of Cu and W, which leads to electromigration-induced chip failure [8–13]. Barrier and capping engineering can help in mitigating electromigration to some extent

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[14]. However, in advanced technology nodes, where the current density in interconnects can at times skyrocket to more than an order of magnitude larger than the current capacity of Cu and W, maintaining the chip reliability becomes a daunting challenge.

Therefore, for advanced nodes, alternative conductors are required, which not only match or exceed the performance of Cu or W, but are also superior to them in reliability. Nanocarbons such as single-walled carbon nanotube (SWCNTs), multi-walled carbon nanotubes (MWCNTs), and graphene are promising materials to replace Cu and W at advanced technology nodes due to their superior electrical and thermal properties as well as higher tolerance to electromigration. SWCNTs in the form of individual nanotubes or a bundle of SWCNTs have been evaluated as interconnects [15–26]. However, the primary challenge is controlling the chirality of SWCNTs to result in either metallic or semiconducting properties. For interconnect applications, it is necessary that metallic SWCNTs are used. MWCNTs have also been actively considered as interconnect materials as they are generally metallic from most growth methods [26]. For horizontal interconnects, precisely aligned growth remains a challenge along with the higher contact resistance due to side contact with metal electrodes [27–31]. In general, nanocarbons face critical challenges when contacting with other materials [32–34], due largely to imperfect interfaces, as well as Fermi level differences and metal–CNT interface chemistry. And the resulting high contact resistance severely degrades their performance. Despite such challenges, their superior properties and potentially high technological return on investment demand a rigorous assessment of nanocarbons as functional interconnect materials for advanced technology nodes, based on our current understanding of their properties.

CNT via interconnects have been investigated extensively in recent years with various approaches, including transport studies, CNT growth engineering, and assessment of CMOS process compatibility [35–48]. The primary process consideration has been the CNT growth temperature being less than 400 °C to be compatible with back-end-of-line processes in the current technology nodes, so that the doping profiles inside the transistors are not affected by the CNT growth cycle [49–51]. For SWCNTs, as stated previously, it is also necessary to grow them with metallic chirality with an areal density of $\sim 10^{13}/\text{cm}^2$. However, for MWCNTs, chirality factor is not as stringent and it has been predicted that a MWCNT via with areal density of $8 \times 10^{12}/\text{cm}^2$ can achieve electrical performance comparable to that of Cu, assuming ballistic transport inside the CNTs [52–55]. Toward this end, there have been studies with catalyst engineering approaches to increase the MWCNT areal density inside vias and use a contact metal with suitable work function to achieve lower contact resistance [56]. While lower contact resistance was achieved, the MWCNT resistivity still remained two to three orders of magnitude higher than that of Cu [57]. A recent report described using Ti as top contact metal with tip-growth MWCNTs in which the catalyst particle sits on top of MWCNT after growth so that it makes contact with all shells [49]. This approach is in stark contrast to other proposed techniques in which catalyst was removed during the planarization step after CNT growth and before contact metallization [57]. The studies reported so far have been focused on fabrication and electrical characterization of CNT vias, but there have been few assessments of both the performance and reliability of CNT vias for advanced technology nodes [58].

In this paper, we review recent studies that examined the performance of vertical CNT via interconnects with linewidths down to 60 nm. Further, based on experimental data for these vias and for individual CNTs, the resistance of 30 nm via is deduced [59]. This via linewidth is similar to that used in the first on-chip interconnect layer for sub-30 nm technology nodes [2]. Therefore, study of 30 nm CNT via performance and reliability provides a suitable benchmark of CNT interconnect performance for potential inclusion in next-generation IC technologies.

2. Test structures for CNT Via interconnects

To evaluate the performance of CNT vias at 30 nm technology node and beyond, two parallel approaches are used. One involves direct probing of individual vertically aligned CNTs to extract contact resistance and CNT resistivity. These extracted values are then used to predict the resistance of a close-packed 30 nm CNT via. The second approach utilizes fabricated CNT vias with widths ranging from 150 nm to 60 nm and their measured resistances to extrapolate the resistance of a 30 nm via. Comparison of via resistances obtained from these two approaches will elucidate the effects of variations in CNT areal density and top contact morphology among vias. The current capacities of individual CNTs and CNT vias are also determined to assess and contrast their reliability behaviors.

2.1. Test structure for individual CNT measurement

Vertically aligned CNTs are grown on a 4" p-type Si wafer at 700 °C using a plasma-enhanced chemical vapor deposition (PECVD) process described in detail elsewhere [60]. The growth time is set for 10 min in order to achieve 1 μm -long CNTs to allow sufficient margin for subsequent mechanical polishing. After CNT growth, to facilitate electrical probing, maintaining rigidity in individual CNTs is needed. Hence, epoxy is deposited as a filler material between CNTs and the sample is subsequently mechanically polished to planarize the surface, removing the catalyst particles at the tips and exposing CNT shells to make direct contacts with the nanoprobe. The Ti underlayer is exposed in an area of the sample to provide a low-resistance ground contact. Fig. 1(a) shows a cross-sectional schematic of the test structure along with an electrical measurement setup, (b) the corresponding scanning electron microscopy (SEM) image of a sample undergoing nanoprob- ing, and (c) a cross-sectional transmission electron microscopy (TEM) image of CNTs [34].

2.2. Test structure for CNT via measurement

For this experiment, vias with different widths ranging from 150 nm down to 60 nm and height of 130 nm are fabricated and patterned on a 4" silicon wafer [59]. A 1 μm -thick thermal oxide film is grown to provide isolation from substrate conduction. A 300 nm thick Cr film is evaporated and then annealed at 400 °C for one hour under nitrogen ambient to reduce the grains and smoothen the film surface, resulting in sheet resistance ranging from 3.2 Ω/\square to 1.1 Ω/\square . To fashion the vias, a 90 nm oxide film is formed on the Cr underlayer followed by a 50 nm layer of amorphous silicon (a-Si) using PECVD. In patterning the vias, a-Si is used as a hard mask to achieve vertical sidewalls. Vias with widths of 150, 120, 90, and 60 nm are obtained with electron beam lithography and reactive ion etching.

Before growing CNTs inside the fabricated vias, blanket deposition of a Ni film is first performed using e-beam evaporation. Using mechanical polishing, the Ni film deposited on the field oxide is removed to allow selective CNT growth inside vias. The sample is then subjected to the same PECVD process for CNT growth, as described elsewhere [59,60]. The growth process is set for 90 s to ensure that CNT tips are protruding above the via edge. In order to fill the space between CNTs with a dielectric and provide rigidity for nanoprob- ing, Al_2O_3 is deposited using atomic layer deposition. To planarize the sample, focused ion beam is used at a glancing angle to remove the protruding section of CNTs to achieve the same length as the via height of 130 nm. The average areal density of CNTs in vias thus obtained is $2 \times 10^{11}/\text{cm}^2$ [59]. The test structure schematic and corresponding SEM image are shown in Fig. 2(a) and (b), respectively, and a cross-sectional TEM image of a 60 nm CNT via is shown in Fig. 2(c). The TEM image confirms no sidewall CNT growth, which is critical for via interconnect applications.

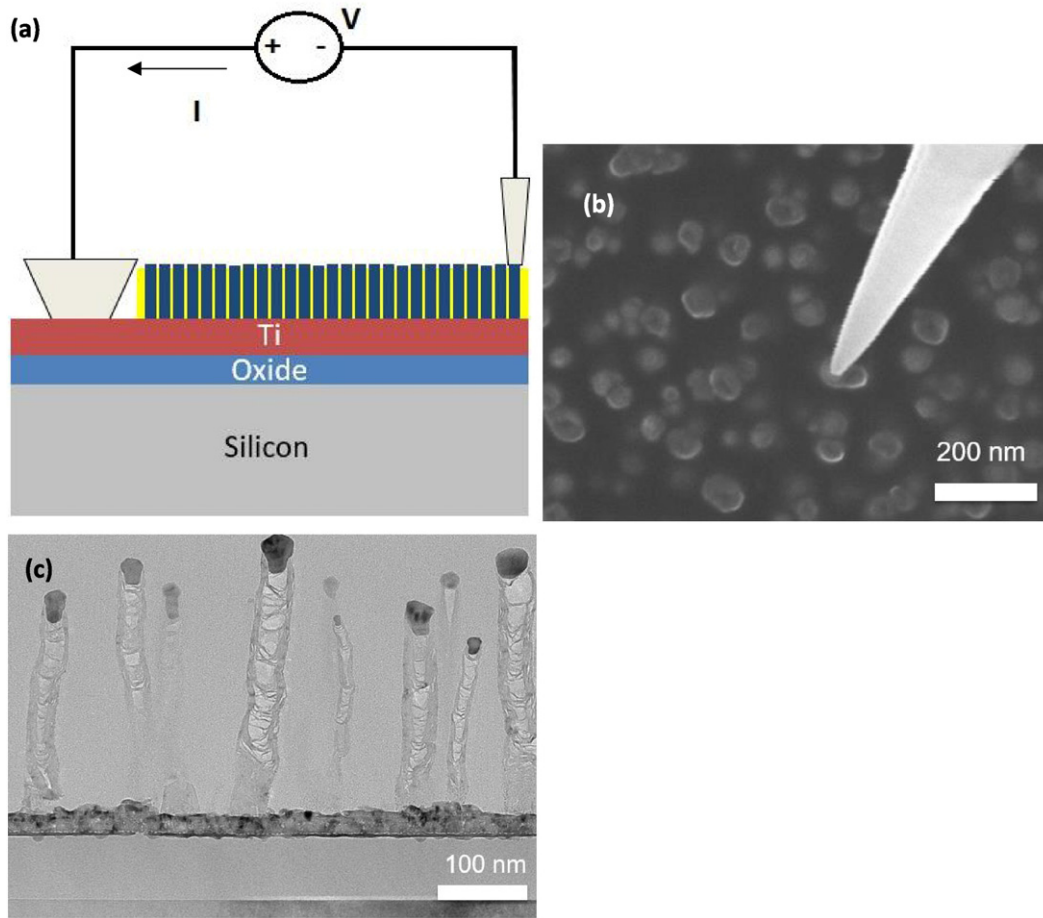


Fig. 1. (a). Cross-sectional schematic of test structure for probing individual CNTs. (b) SEM top-view image after initial landing of nanoprobe on tip of CNT which is embedded in epoxy. (c) Cross-sectional TEM image of CNTs. CNT structure consists of cup-shaped graphitic planes.

3. Electrical characterization

Electrical characterization to determine resistance and current capacity of individual CNTs and CNT vias is carried out using 2-point probe measurement technique with a nanoprobe inside the SEM chamber. Accurate determination of CNT current–voltage (I – V) behavior requires stray contributions from probe pads to be minimized, hence direct contact with CNTs and CNT vias is made using W nanoprobes. Exposed underlayer metal is used as ground electrode instead of a large array of CNTs or CNT vias. This setup has the advantage of reducing parasitic resistances due to the absence of pads and lines connecting pads to devices. And the resistance contributions from probes and underlayer metal can be de-embedded from the total measured resistance. Hence, accurate extraction of via and CNT parameters is attainable, which in turn leads to the projection of 30 nm CNT via resistance.

3.1. Individual CNT probing

Individual vertically aligned CNTs with a diameter of 50 nm are selected from the blanket grown sample and probed to obtain the I – V characteristics and resistance for each CNT. CNTs with five different heights or lengths are probed in situ in a high-vacuum scanning electron microscope (SEM) chamber to generate resistance vs length data. A schematic of the measurement setup and a SEM image of a nanoprobe in contact with a CNT are shown in Fig. 1(a) and (b), respectively. Accurate measurement of individual CNT resistance requires a stable and mechanically robust contact to be made between CNT and W probe. In

order to facilitate a stable contact with the cross-section of an individual CNT, the following procedure is used. Ambient exposed CNT shells have atmospheric impurities adsorbed on them which can damage the CNT if a current spike occurs at the interface. Therefore, a 60 nm-diameter nanoprobe with an applied voltage of 2.5 V and current compliance of 50 nA is slowly brought into contact on top of the CNT with the help of piezo actuators, while the ground probe is resting on the underlayer metal. Once a stable contact is established between CNT and nanoprobe, the current reaches compliance and the voltage drops and remains stable. After making initial contact, the I – V behavior is measured and the resistance (reciprocal slope of I – V curve at zero voltage) is obtained, which is usually tens of k Ω or higher. Further, the initial I – V behavior is generally not linear. Ambient exposure causes atmospheric impurities to be adsorbed on the CNT [61] and thermal treatment is required to desorb these impurities in order to obtain accurate I – V behavior. Such treatment is provided by Joule heating with current stressing of the CNT in multiple cycles. After each stress cycle, the resistance is recorded. If the stress current reaches a value at which the current density exceeds the current capacity, the CNT breaks down. Thus the resistance is carefully monitored such that no further stressing is applied when its value starts to stabilize.

Fig. 3(a) shows the I – V plot of an individual 50 nm CNT before and after 3.5 mA of current stressing and Fig. 3(b) shows the resistance versus current stressing behaviors for two devices up to breakdown. The current capacity for either device is in excess of 10^8 A/cm². For each of the five lengths, 4 to 7 CNTs are probed to yield a resistance versus length plot as shown in Fig. 3(c) [34]. Besides the CNT and CNT-metal contacts, the measured total resistance consists of contributions from

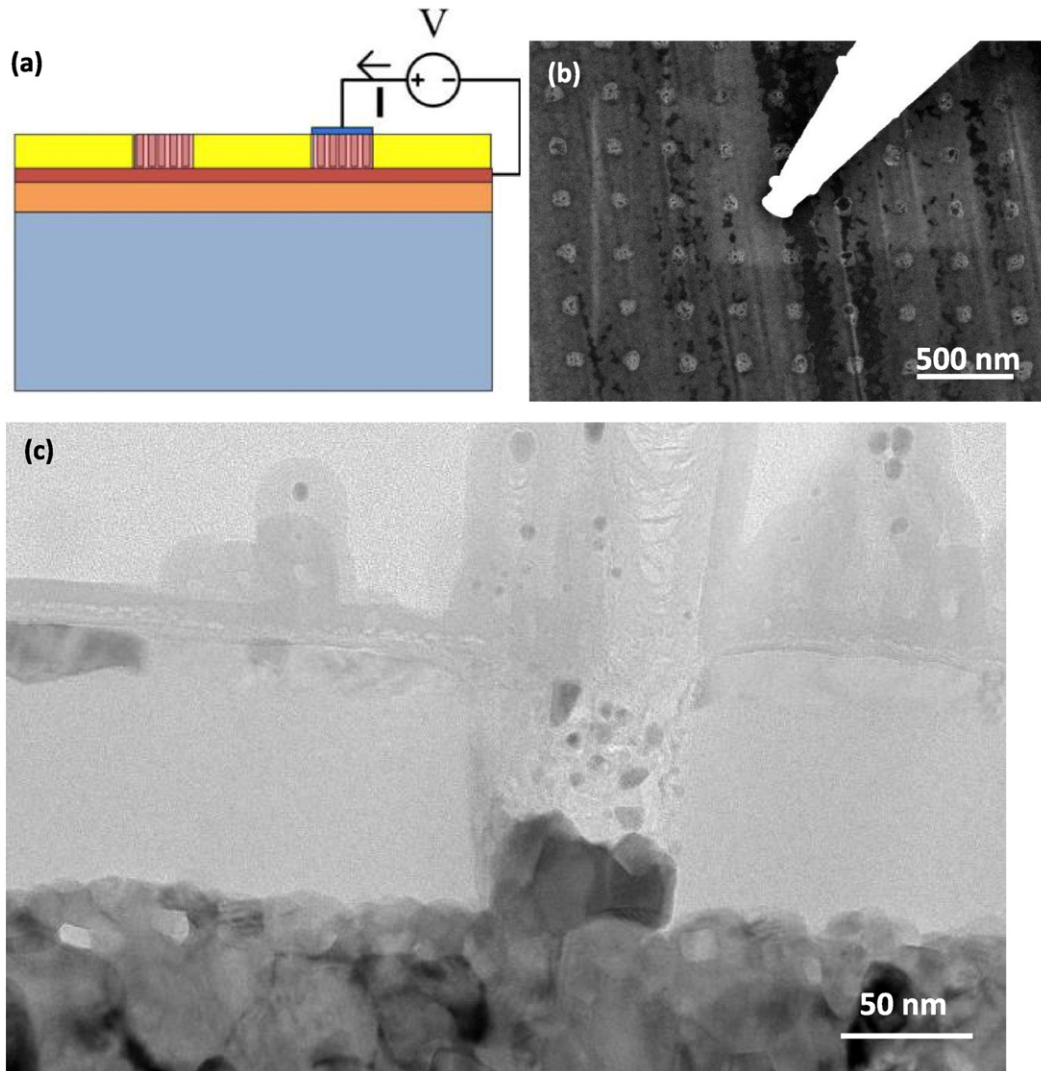


Fig. 2. (a) Cross-sectional schematic of test structure for CNT via for electrical probing. (b) SEM top-view image with a nanoprobe in contact with a single 60 nm via. (c) Cross-sectional TEM image of an individual 60 nm CNT via after Al_2O_3 filling but before polishing [59]. No CNT growth from sidewalls is observed. Some CNTs will not contribute to conduction upon polishing and probing, as the Ni particles at the tips of those CNT are embedded below the via edge. Also, due to the high growth temperature, the Cr underlayer experienced local melting and protrudes up the via as a result of capillary force.

the underlayer metal, probe-metal contact, and probes. In order to de-embed these resistance contributions, the nanoprobes are contacted directly with the underlayer metal, and the resulting resistance is subtracted from the total resistance.

3.2. CNT via probing

Individual vias each containing a collection of CNTs are measured using a nanoprobe in direct contact with the top of the via and another on the underlayer metal, as shown schematically in Fig. 2(a). A SEM image of an array of vias showing a nanoprobe making contact with one via is given in Fig. 2(b). Electrical measurement of vias is similar to that described in Section 3.1 for individual CNTs. Resistances are recorded after sufficient current stressing for vias with cross-sectional widths of 150 nm, 120 nm, 90 nm, and 60 nm. Typical I–V characteristics of a 60 nm via before and after current stressing are shown in Fig. 4(a) and the resistance versus stress current behaviors of two vias are shown in Fig. 4(b). The current capacity of either via is about 2×10^7 A/cm², less than that for the 50 nm CNTs as expected, since the average diameter of the CNTs inside the 60 nm via is only ~15 nm. Multiple devices for each via width are probed and the via

resistance versus width data are plotted in log–log scale for subsequent analysis and parameter extraction [59].

4. Results and discussion

Electrical characterization to extract contact resistance, resistivity, and current capacity are performed on both set of samples. For probing individual CNTs each with 50 nm diameter, the resistance versus length plot is shown in Fig. 3(c). The total device resistance is given by.

$$R_{\text{Total}} = R_c + R_{\text{CNT}} = R_c + 4\rho \times L_{\text{CNT}} / (\pi D_{\text{CNT}}^2), \quad (1)$$

where ρ is the CNT resistivity, L_{CNT} the CNT length, and D_{CNT} the CNT diameter. R_c consists of not only the CNT-underlayer metal and CNT-probe contact resistances, but also includes the contributions from the underlayer metal, probe-metal, and probes. Based on Eq. (1), a linear regression on the data is performed. The resistance intercept of the linear fit yields $R_c = 390 \Omega$ for a CNT with a diameter of 50 nm. From the slope of the linear fit and Eq. (1), a CNT resistivity of $2.3 \times 10^{-4} \Omega \text{ cm}$ is obtained.

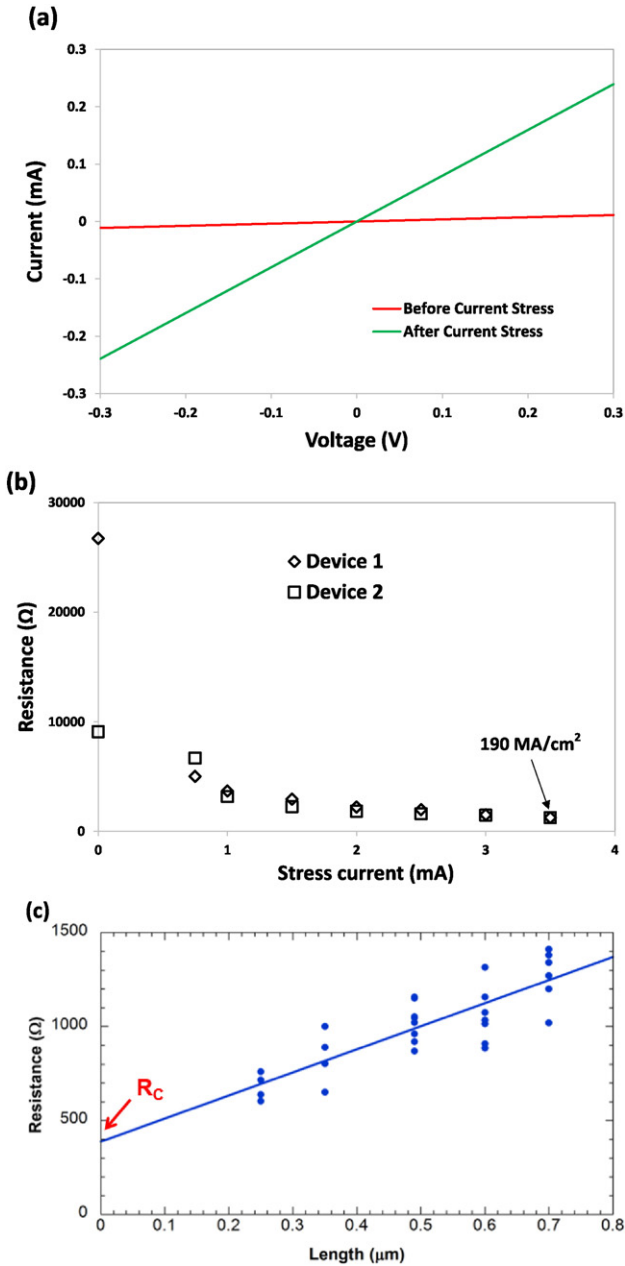


Fig. 3. (a). CNT I–V characteristics before and after 3.5 mA current stressing. Resistance is improved by two orders of magnitude after current stressing. (b) Resistance vs stress current behaviors of two 50 nm CNTs. Both are stressed up to 3.5 mA resulting in a current carrying capacity of 190 MA/cm². (c) Resistance vs length plot for individual CNTs to extract CNT resistivity and contact resistance R_c [34].

Further, R_c can be expressed as.

$$R_c = R_{\text{CNT-underlayer}} + R_{\text{CNT-probe}} + R_{\text{underlayer}} + R_{\text{probe-metal}} + R_{\text{probes}} \quad (2)$$

The last three components in Eq. (1) are independent of CNT contacts and can be lumped together as R_m and extracted by probing the underlayer metal with nanoprobes, resulting in

$$R_c = R_{\text{CNT-underlayer}} + R_{\text{CNT-probe}} + R_m \quad (3)$$

After subtracting R_m , the contact resistance becomes 230 Ω for an individual CNT with a diameter of 50 nm. This is the true contact resistance with contributions from CNT bottom and top interfaces with metals.

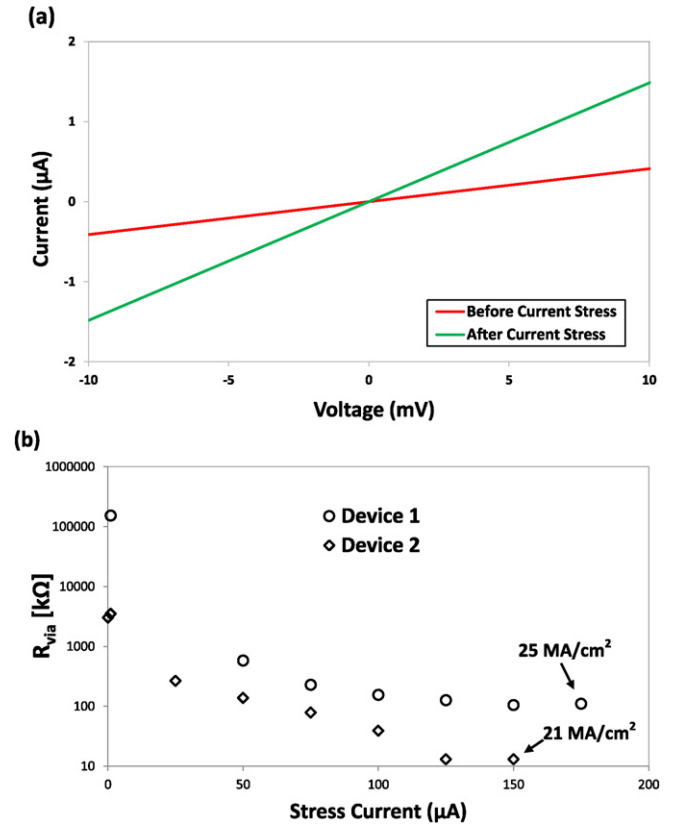


Fig. 4. (a). I–V characteristics of 60 nm CNT via before and after current stressing. (b) Resistance vs stress current behaviors for two 60 nm CNT vias. A CNT fill factor of 20% obtained from SEM image analysis is used to compute the indicated current density for each device right before breakdown. Current capacity of either via is more than an order of magnitude higher than those of Cu and W.

For via applications, it is important to grow CNTs at as low a temperature as possible [49–51]. Lowering the growth temperature generally results in more defects in the CNT structure and at and/or near the interface with the underlayer metal, thus increasing the via resistance. The resistivity obtained by probing individual CNTs is an order of magnitude lower than those for CNTs grown at lower temperatures [49,51]. Also, the contact metals, Ti underlayer and W probe, for measuring individual CNTs have relatively small work function difference with CNT, which accounts for the low contact resistance [56].

The CNT resistance versus length plot shown in Fig. 3(c) exhibits a strong length dependence, indicating that the electron mean free path is most likely less than the shortest CNT length measured, 250 nm, as opposed to the ideal case of 1000 nm or more [29]. Mean free path can be directly extracted from resistance versus length data [62], where the resistance becomes independent of length when the CNT length falls below the mean free path. The mean free path of electrons in CNT extracted was 24–74 nm [62]. While mean free path in CNTs is influenced by many factors, such comparison of our result with others supports our analysis of individually probed CNT resistance data.

To examine the CNT-underlayer metal interface, nanostructural analysis of individual CNTs is performed using TEM, with the result shown in Fig. 1(c) [34]. It is observed that the CNT interior is not hollow but consists of cup-shaped graphene planes forming a bamboo-like structure. A high-resolution image of the CNT-underlayer metal interface shown in Fig. 5 reveals graphitic planes nearly perpendicular to the metal surface [34].

To further examine the CNT nanostructure and its dependence on growth temperature, Raman spectroscopic analysis is performed for three different growth temperatures. Normalized Raman data with respect to G band is shown in Fig. 6, where G-band corresponds to

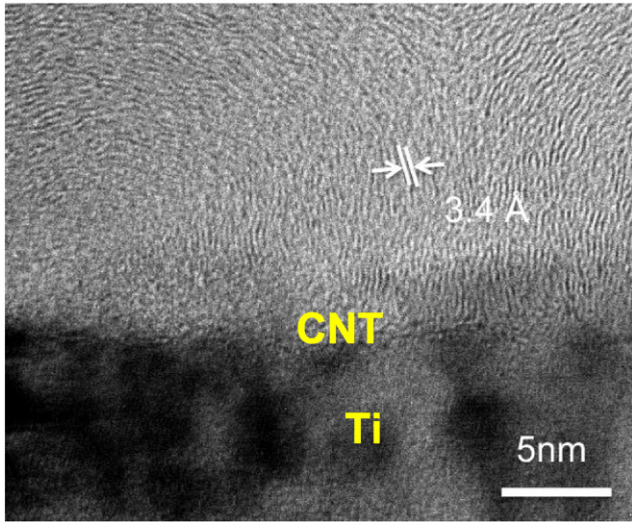


Fig. 5. Cross-sectional TEM image of CNT-underlayer metal interface. Graphene planes are nearly perpendicular to the metal surface. Interplanar spacings match well with that of graphite [34].

Raman active mode of graphitic materials, D-band corresponds to defect band, and G' is the second harmonic of G band. For CNT growth at 700 °C, the D/G ratio is 0.9 with distinctive sharp D and G peaks. The D band originates from a hybridized vibrational mode associated with graphene edges and it indicates the presence of some defects in the graphene layers, most likely due to the bamboo or cup-shaped structure inside each CNT, as illustrated by the TEM image in Fig. 1(c). As the CNT growth temperature is reduced, the D/G ratio doesn't change, while the G and D peaks are not as sharp but appear to be modulated by second-order modes, and the G'/G ratio increases indicating deviations from graphitic characteristics [51]. With decreasing growth temperature, low intensity peaks appear at the 700 (cm^{-1}) indicative of presence of a-C phase. Therefore, perhaps even higher growth temperature is needed to yield high-quality CNTs for interconnect applications, despite the thermal budget requirements for Si chip manufacturing. Moreover, as shown in Fig. 3(b), individual CNTs are intact up to 190 MA/cm^2 , which is at least two orders of magnitude more reliable than Cu or W, making CNTs particularly appealing for sub-30 nm technology nodes.

For CNT via measurements, different widths with the same length are probed. The via resistance versus width plot in log–log scale is shown in Fig. 7 [59] and a statistical linear regression is performed to

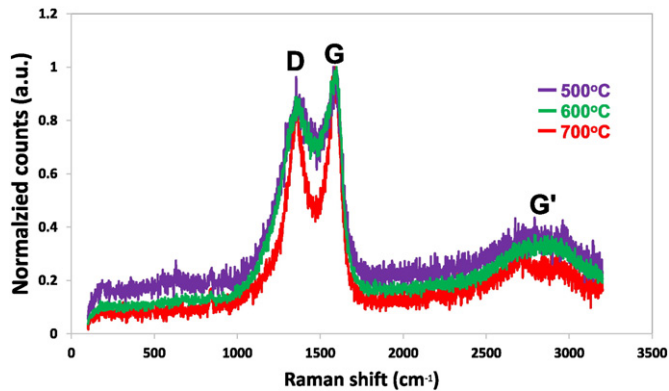


Fig. 6. Raman analysis of blanket grown CNTs at 500 °C, 600 °C, and 700 °C. Lowering the growth temperatures results in increasing defect (D band intensity) and also the peaks are less sharp.

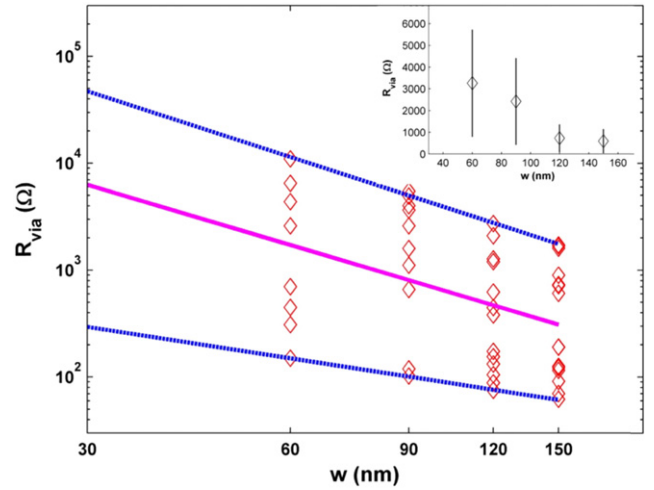


Fig. 7. Log–log plot of resistance vs via width for CNT vias [59]. Statistical linear regression yields a slope of -1.9 compared to a slope of -2 based on Eq. (6). Projected resistance for 30 nm via from average linear fit is 5.7 k Ω , and 295 Ω from the best fit. The average via resistance (data point) and standard deviation for each width (vertical bar) are given in the inset.

project the resistance for a 30 nm via. Similar to the analysis for individual CNT data, the via resistance is expressed as

$$R_{\text{via}} = R_{\text{Cr}} + R_{\text{probe}} + R_{\text{probe-Cr}} + R_{\text{probe-CNT}} + R_{\text{Cr-CNT}} + R_{\text{CNT}}. \quad (4)$$

R_{Cr} , R_{probe} , and $R_{\text{probe-Cr}}$ denote the resistances of the Cr underlayer, nanoprobes, and the probe-Cr contact resistance, respectively. Their sum R_m is estimated by measuring the resistance between two nanoprobes landed on the Cr underlayer, yielding $\sim 15 \Omega$ for a probe-to-probe distance of $\sim 10 \mu\text{m}$. $R_{\text{Cr-CNT}}$ and $R_{\text{probe-CNT}}$ make up the total contact resistance R_C , and R_{CNT} is the CNT resistance. Accordingly, the CNT via resistance becomes.

$$R_{\text{via}} = R_m + R_C + R_{\text{CNT}}.$$

To evaluate the contribution of R_C , we assume that the CNT-metal resistance is constant and about the same as the extracted contact resistance between a single 50 nm-diameter CNT and metal, $R_{\text{ci}} = 230 \Omega$, obtained above. This is probably an underestimate as the average CNT diameter inside a typical via with 60–150 nm widths is 10–15 nm. R_C can then be estimated by dividing R_{ci} by the number of CNTs inside the via making contact with the nanoprobe, which is the product of CNT areal density D_{CNT} ($\#\text{CNTs}/\text{cm}^2$) and via cross-sectional area w^2 , i.e. $R_C = R_{\text{ci}} / (D_{\text{CNT}} \times w^2)$. Assuming ohmic conduction along the height h of each CNT, we obtain

$$R_{\text{via}} = R_m + R_{\text{ci}} / (D_{\text{CNT}} \times w^2) + \rho_{\text{CNT}} \times h / (D_{\text{CNT}} \times w^2 \times A_{\text{CNT}}). \quad (5)$$

Since R_m is at least one order of magnitude lower than R_{via} , it is neglected in rewriting Eq. (5) as

$$\log(R_{\text{via}}) = \log[R_{\text{ci}} / D_{\text{CNT}} + \rho_{\text{CNT}} \times h / (D_{\text{CNT}} \times A_{\text{CNT}})] - 2 \log(w). \quad (6)$$

The log–log plot of via resistance versus width in Fig. 7 results in a slope of -1.9 for the average linear fit, compared to -2 based on Eq. (6). This result strongly supports the methodology used in this analysis.

To project resistances vias with widths 30 nm or less using the data in Fig. 7, a best-case value of 295 Ω and an average value of 5.7 k Ω are obtained for a via with width 30 nm and length 130 nm, by extrapolating the respective fitted straight lines in Fig. 7. Using information obtained from individual CNTs, resistance of 30 nm CNT via can be

Table 1

Comparisons of 30 nm CNT via properties based on reported values and projections. Comparisons with Cu and W are also included. For projected via resistance using data from individual CNTs, square close-packing of four 15 nm CNTs is assumed.

Via	R_c (Ω)	ρ (Ω -cm)	D_{CNT} (nm)	CNT resistance (Ω)	CNT density ($\#/cm^2$)	30 nm \times 130 nm via resistance	Current capacity (MA/cm ²)
Individual CNTs [34]	2555	2.3×10^{-4}	15	1692	4.4×10^{11}	1.1 k Ω (projected)	190
Sub-150 nm vias [59]	NA	NA	~10	NA	2.1×10^{11}	5.7 k Ω (extrapolated)	21–25
Cu	15	5×10^{-6} [67]	NA	NA	NA	25 Ω (projected)	2.5 [64]
W	5	3.8×10^{-5} [67]	NA	NA	NA	60 Ω (projected)	1 [65]
30 nm via [58]	NA	NA	15	7.8 k	1.5×10^{11}	6.7 k Ω (measured)	400
70 nm via [68]	NA	NA	10	52	3×10^{11}	262 Ω (projected)	500

estimated as follows. Starting with CNTs each with a diameter of 15 nm, four identical close-packed CNTs are placed in a square arrangement in a 30 nm via, which has an areal density of $4.4 \times 10^{11}/cm^2$, about two times higher than that obtained for the grown CNT grown inside vias. Then, from the CNT resistivity extracted and assuming it is constant for all CNTs grown on the same wafer regardless of their diameters (unlike Cu and W), the resistance of a 15 nm CNT with length of 130 nm is calculated to be 1.7 k Ω , which does not include contact resistance. To calculate the contact resistance of a 15 nm CNT from individually probed CNTs with diameter 50 nm, the extracted contact resistivity of the 50 nm CNT is used, resulting in 2.6 k Ω . Thus, the total resistance of the 30 nm CNT via containing four identical 15 nm CNTs is 1.1 k Ω . This value is less than the average projected 30 nm via resistance of 5.7 k Ω but higher than the best-case value. Thus the two approaches yield reasonable agreement considering the fact that the measured CNT areal density inside vias is less than that of the close-packed arrangement, and taking into account the variations in CNT diameter and data spread due to large variations in the via top contact [59].

As given in Table 1, the published projected and extrapolated values for 30 nm CNT vias are all much higher than their Cu and W counterparts, due to higher resistivity and contact resistance. While the CNT resistivity extracted from our measurements is about 40 times that of bulk W and two orders of magnitude higher than bulk Cu, contact resistance is the dominant factor contributing to total via resistance. Nevertheless, by increasing CNT areal density and decreasing average CNT diameter, via resistance can be reduced significantly. Also, lower contact resistance can be achieved with improved CNT growth and via fabrication processes, as well as top via contact metallization [34].

Another critical component of via interconnect electrical properties is its current capacity which dictates the reliability of the eventual functionalized device. Our results as well those reported by others given in Table 1 show that CNTs have much higher current capacity than Cu or W. While Fig. 4(b) shows that a CNT via remains intact up to a current density of 25 MA/cm², individual CNTs can withstand currents almost ten times higher, as shown in Figs. 3(b). The primary factor for high current capacity is the strong sp² C–C bonding and absence of grain boundaries unlike all conventional metal deposits such as Cu and W interconnects that give rise to electromigration-induced failure. However, CNTs are susceptible to breakdown due to Joule heating [63], which can be exacerbated by the presence of oxygen [61]. In the CNT via structure, aluminum oxide has been used as a filler which can serve as an oxygen source, suggesting a possible explanation for the lower CNT via current capacity than that of individual CNTs which are embedded in a hydrocarbon polymer and probed under high vacuum. Another possible cause for the lower current capacity of CNT vias is the confined via structure with less paths for heat dissipation than in the sample of blanket-growth CNT arrays. Nevertheless, even the lowest recently reported CNT current capacities are at least an order of magnitude higher than those of bulk Cu and W, which are even lower in the nanoscale [64,65]. Therefore, the main challenge for functionalizing CNT via interconnects remains in improving their performance, namely, lowering the via resistance to at least that of W for the same linewidth, so that CNT can be seriously considered as a replacement via interconnect material for next-generation chip manufacturing [2,66].

5. Conclusions

Electrical characterization of CNT via interconnects has been carried out using two parallel approaches, by measuring individual CNTs and sub-150 nm CNT vias, respectively. Resistances of 30 nm via are projected using both approaches and are in reasonable agreement considering the variations of contacts and CNT densities among vias. However, even the best projected resistance values for 30 nm CNT via are still much higher than those for its Cu and W counterparts. In the sub-20 nm IC technology nodes, typical first-level via has an aspect ratio of 10 (height-to-width) [2]. Therefore, based on results reported here and by others, almost defect-free CNTs are needed to increase the mean free path so that near-ballistic transport is achieved in these small structures. The aspect ratio of the CNT vias with the best reported performance is less than 1 which is not a realistic solution [66]. However, the reported results were for devices fabricated at temperatures compatible with the thermal budgets at advanced nodes. When a higher aspect ratio was used, it was difficult to grow high-quality CNTs inside the via [57]. In short, the primary challenges limiting the electrical performance of CNT via interconnects are: a) growth in high aspect ratio structures, b) minimum defects in CNTs so that near-ballistic transport can be achieved, which can in turn lessen the dependence of resistance on CNT height, c) higher CNT packing density inside the via to reduce the metal–CNT contact resistance, and d) top via contact engineering. Therefore, improved CNT growth and via fabrication processes are needed.

On the other hand, the CNT current capacity has been shown to far exceed those of both Cu and W, and can undoubtedly be enhanced further as the CNT growth and via fabrication processes improve. The reported current capacity, while significantly higher than both Cu and W, is about an order of magnitude less than the highest value reported [58]. This difference can be attributed partly to less heat dissipation through the both the oxide filler inside the via and surrounding dielectric in our CNT via sample. Also, defects in the CNT can significantly impact its current capacity. Thus, in realizing the usage of CNT as via interconnect material for chip manufacturing, the reliability problem has at least been solved in principle, but the via performance remains a critical challenge in the coming years.

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