A Unified RLC Model for High-Speed On-Chip Interconnects

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***Abstract*—In this paper, we propose a compact on-chip interconnect model for full-chip simulation. The model consists of two components, a quasi-three-dimensional (3-D) capacitance model and an effective loop inductance model. In the capacitance model, we propose a novel concept of effective width (W_{eff}) for a 3-D wire, which is derived from an analytical two-dimensional (2-D) model combined with a new analytical "wall-to-wall" model. The effective width provides a physics-based approach to decompose any 3-D structure into a series of 2-D segments, resulting in an efficient and accurate capacitance extraction. In the inductance model, we use an effective loop inductance approach for an analytic and hierarchical model construction. In particular, we show empirically that high-frequency signals (above multi-GHz) propagating through random signal lines can be approximated by a quasi-TEM mode relationship, leading to a simple way to extract the high-frequency inductance from the capacitance of the wire. Finally the capacitance and inductance models are combined into a unified frequency-dependent RLC model, describing successfully the wide-band characteristics of on-chip interconnects up to 100 GHz. Non-orthogonal wire architecture is also investigated and included in the proposed model.**

***Index Terms*—Capacitance, high-speed integrated circuits, inductance, modeling, on-chip interconnects.**

I. Introduction

As COMPLEMENTARY metal oxide semiconductor (CMOS) technology advances into nanometer feature size and multi-GHz frequency regime, on-chip interconnect delay and signal integrity are becoming major concerns in integrated circuit design [1]. A holistic prescription to overcome the on-chip interconnects limit, as well as an accurate understanding and modeling of the wires has become more critical than ever. In particular, the growing complexity and tight design margin of today's ULSI systems require a compact yet accurate on-chip interconnect model for fast full-chip-level extraction.

In on-chip interconnect modeling, the different behaviors of capacitance and inductance must be taken into consideration. Since electrostatic interaction between wires is very short-range, consideration of only nearest neighbors provides sufficient accuracy for capacitance extraction. However, capacitance is a sensitive function of geometry, making any closed-form modeling for general three-dimensional (3-D) wires a formidable task. Therefore quasi-3-D (Q-3-D or 2.5D) modeling [2]–[4] has become a promising approach to alleviate the difficulty of a pure 3-D model. The major challenge in Q-3-D model is how to decompose a 3-D structure into two-dimensional (2-D) segments and include effects of the fringing electric field between adjacent 2-D segments. Here we propose a convenient concept, an effective width of a crossing wire, to provide an efficient and physics-based scheme for the decomposition. To provide sufficient accuracy for deep sub-micron technology, 3-D wall-to-wall fringing capacitance as well as 2-D fringing capacitance is incorporated in the proposed model.

Unlike an electric field, a magnetic field has long-range interaction. Therefore in inductance extraction, not only nearest neighbors but also many distant wires must be considered. As a consequence, defining current loops or finding return paths becomes a major challenge in inductance modeling. Although partial-inductance-based methodologies [5], [6] have been used to alleviate the difficulty of finding return paths, it is restricted to small structures due to computational burden in solving the resulting dense matrix. In this paper we propose an effective loop inductance model for high-speed on-chip interconnects. We will demonstrate an analytic and hierarchical approach to construct the model. To meet high-frequency demands of today's ULSI systems, we investigate random capacitive coupling effects. Random signal lines as well as power lines can provide return paths through capacitive coupling at high frequencies [7]. With a full-wave solver and an S-parameter-based experiment, we conduct a quantitative investigation of the nonquasi-static effect. In particular, we develop a novel and efficient methodology to model inductance using a quasi-TEM mode of wave propagation.

The capacitance and inductance models are described in Sections II and III respectively, and in Section IV they are combined to yield a frequency-dependent RLC model valid up to 100 GHz. In each part of the modeling, we extend our investigation to nonorthogonal interconnect architecture, which has drawn increased attention [8], leading to a unified model for general nonorthogonal wires.

II. A Quasi-3-D On-Chip Capacitance Model

Although a few pure 3-D models [9], [10] have been proposed, they provide only a part of the overall 3-D capacitance,

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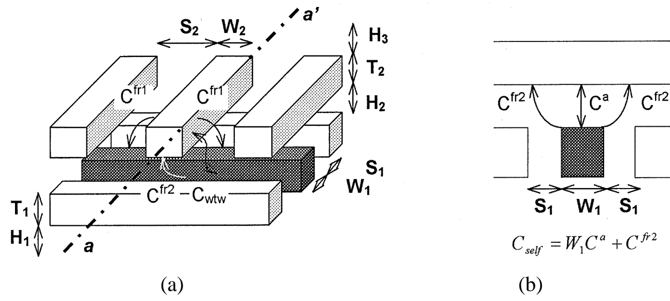


Fig. 1. (a) Generic crossover structure showing various components of C_{cross} and (b) cross-sectional view along aa′. The crossover capacitance (C_{cross}) is composed of an area component (C^a), 2-D fringing components (C^{fr1}, C^{fr2}), and 3-D fringing component (C_{wtw}).

namely, crossover capacitance. Since the total capacitance is composed of intra-layer capacitance (coupling capacitance) and inter-layer capacitance (self capacitance), which change with the influence of neighboring lines, we still need an efficient way to deal with the interaction between neighboring wires in general 3-D structures. To address this issue, we propose a Q-3-D capacitance extraction methodology using an effective width. The effective width, which represents an electrostatic width of the crossover wire, provides a physics-based way to decompose any 3-D structure into a combination of 2-D structures.

A. Effective Width of a 3-D Wire

A generic 3-D crossover structure is shown in Fig. 1(a). The capacitance between an object line and a crossover line, C_{cross}, is composed of four components. Along aa′ of the crossover structure, we can define a 2-D cross section and corresponding capacitance per unit length, C_{self}, between the object line and crossover line, as shown in Fig. 1(b). C_{cross} can then be expressed as the sum of a 2-D capacitance ($W_2 C_{self}$) and additional fringing capacitances ($W_1 C^{fr1}$, C_{wtw})

$$\begin{aligned} C_{cross} &= W_1 W_2 C^a + W_2 C^{fr2} + W_1 C^{fr1} + C_{wtw} \\ &= W_2 C_{self} + W_1 C^{fr1} + C_{wtw}. \end{aligned} \quad (1)$$

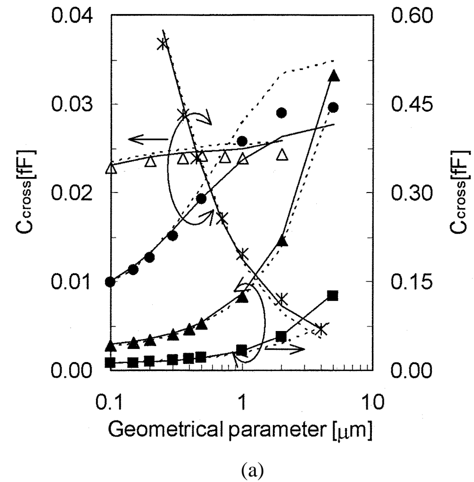
Rearranging the terms, (1) is further simplified into a de facto 2-D form

$$C_{cross} = W_{eff} C_{self} \quad (2)$$

where

$$W_{eff} \equiv W_2 + \frac{W_1 C^{fr1}}{C_{self}} + \frac{C_{wtw}}{C_{self}}. \quad (3)$$

In (2), 3-D crossover capacitance is expressed as capacitance per unit length (C_{self}) multiplied by an effective width (W_{eff}). Fringing fields, which change gradually from the edge of the crossover line, are lumped into W_{eff} defined in (3). We interpret W_{eff} as a lumped electrostatic width of the crossover line. As the wires get more closely packed, becoming taller and thinner with high aspect ratio, the second and third terms on the right-hand-side of (3) become dominant, making the effective width much larger than the physical width. In particular, wall-to-wall capacitance is increasingly critical in today's deep sub-micron wires [11], [12]. A closed-form C_{wtw} is constructed



(a)

	W_1	W_2	S_1	S_2	T_1	T_2	H_1	H_2	H_3
●	.2	.2	.2		.35	.35	.45	.45	.45
✱	.2	.2	.4	.4	.35	.35	.45		.45
△	.2	.2	.4	.4		.35	.45	.45	.45
■	.1		.2	.4	.35	.45	.45	.45	.65
▲	1.		.2	.4	.35	.45	.45	.45	.65

(b)

Fig. 2. Comparison between our model (solid line), Wong's model (dashed line) and 3-D field solver (symbol) for C_{cross}. For each curve and symbol, one parameter is varied with other parameters being fixed as given in the table. The parameter ranges are $0.1 \le W, S \le 5$, $0.1 \le T \le 2$, and $0.25 \le H \le 4$, in μm.

using functional approximation. In W_{eff} calculations, we use Chern's 2-D model [9] with some modifications as well as our C_{wtw} model. Detailed formulas for the 2-D and C_{wtw} models are given in Appendix A. By including the wall-to-wall fringing capacitance model, our crossover capacitance model shows excellent agreement with a 3-D field solver[1] down to the deep sub-micron regime, as shown in Fig. 2. Our results show an average error of 3% and a maximum error of 10%, while Wong's model [10] shows 8% and 35%, respectively, for the range of geometrical parameters shown in the figure.

B. Q-3-D Capacitance Extraction

Since the effective width has the physical meaning of an electrostatic width, we use it instead of physical width when we decompose any general 3-D structure into a combination of contiguous 2-D segments, as illustrated in Fig. 3. Each 2-D segment belongs to one of four distinct cross sections, as defined in Fig. 3(c), and is completely described by the 2-D capacitance model (C_i) as outlined in Section II-A. Here C_i includes coupling capacitance to parallel neighbors (C_{couple}) as well as self capacitance to crossing neighbors (C_{self}). Generally, C_i is represented by a matrix to describe the components. The total capacitance of the object line (C_{total}) is determined by simply adding the capacitances ($C_i W_i$) from each 2-D segment

$$C_{total} = \sum_i W_i C_i \quad (4)$$

where W_i denotes the actual width of the ith segment as defined by W_{eff} of each crossing line.

[1]"Maxwell Spicelink," from ANSOFT.

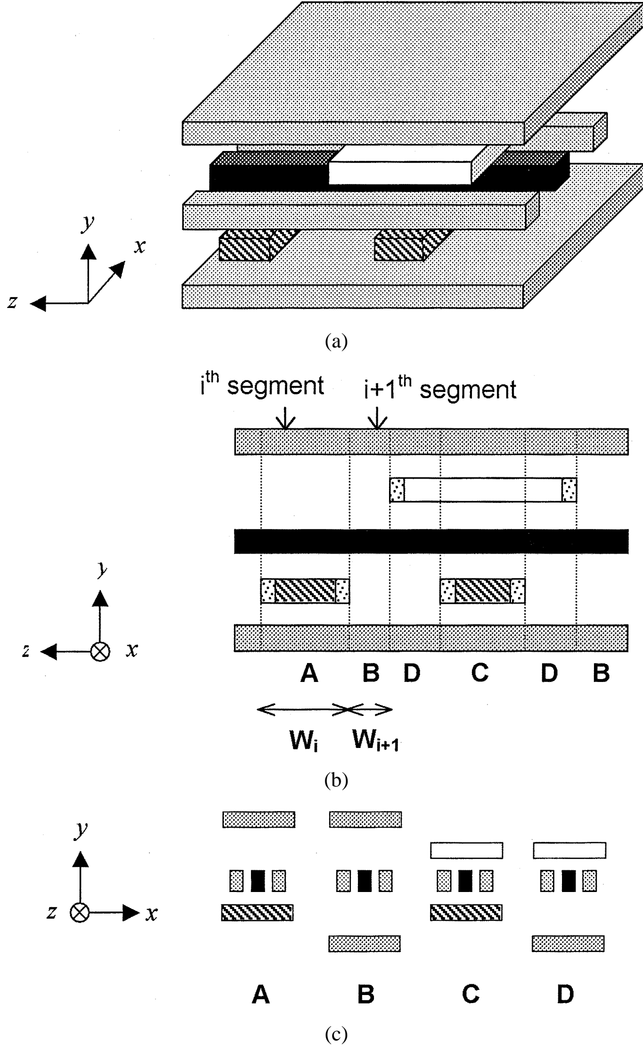


Fig. 3. Typical 3-D structure (a) showing segmentation with W_{eff}. In the cross section along the object line, the 3-D structure is divided into contiguous segments (b), which belong to one of the four cross sections as defined in (c). In (b), W_{eff} of each crossover line defines the actual width (W_i or W_{i+1}) of the relevant segment used to obtain the total capacitance.

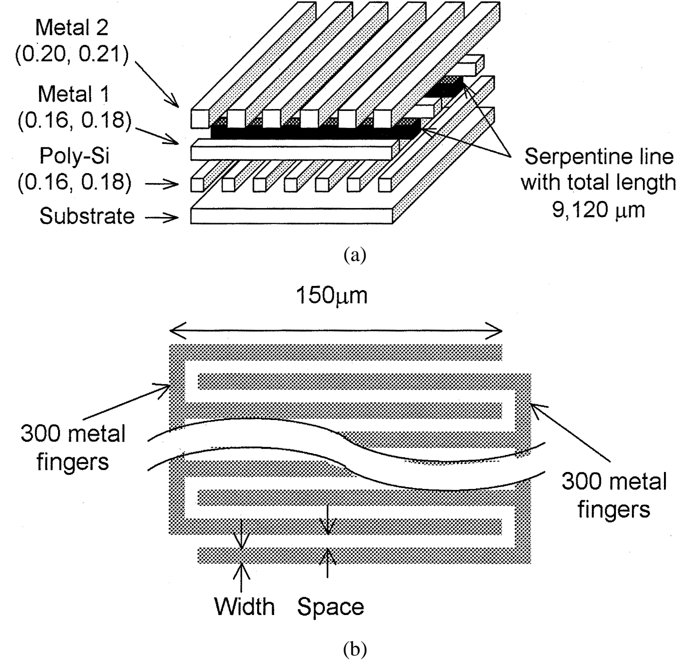


Fig. 4. Test structures used to confirm the proposed Q-3-D capacitance model. (a) Serpentine line structure (bird's eye view). All the wires except the black object wire (SP1) are grounded. Width and space of each layer are shown in parenthesis in μm unit. (b) Comb-like line structure (top view). Width (=Space) of the interdigitated fingers for Metal 1 (COMB1) and Metal 7 (COMB7) layers are 0.18 and 0.4 μm, respectively.

TABLE I
CAPACITANCE EXTRACTION RESULTS FOR THE STRUCTURE SHOWN IN FIG. 4. ALL THE GROUNDED LINES IN FIG. 4(a) ARE TIED TOGETHER IN THE ACTUAL TEST STRUCTURE BUT ARBITRARY SEPARATED IN FIELD-SOLVER SIMULATION AND OUR MODEL. THEREFORE ONLY C_{total} IS MEASURED FOR FIG. 4(a)

	C[pF]	C_{total}	C_{couple}	C_{self}
SP1	Model	1.83	1.18	0.65
	Field Solver	1.81	1.20	0.60
	Measurement	1.80	NA	
COMB1	Model	8.01	7.09	0.93
	Field Solver	8.03	7.13	0.85
	Measurement	7.89	7.04	0.85
COMB7	Model	11.69	11.47	0.22
	Field Solver	11.79	11.46	0.17
	Measurement	12.43	12.18	0.25

Using the effective width for the segmentation, for example, W_{i+1} in Fig. 3(b) approaches zero while W_i grows substantially as the wires' packing density increases, due to shielding by crossing wires. Since cross section B (W_{i+1}) has larger intra-layer capacitance than cross section A (W_i), previous models [9], [10] using physical width for the segmentation would result in over-estimates of intra-layer capacitance for closely packed wires.

We apply the proposed Q-3-D model to test structures fabricated with a state-of-the-art 0.18 μm technology as shown in Fig. 4. The technology includes a wide range of geometrical parameters for metal layers Metal 1 to Metal 7 and various dielectrics with different dielectric constants.[2] Capacitances for the structures are measured at 100 KHz with a precision impedance analyzer, Agilent 4294 A. The measurement data include the parasitic capacitance of the probing pad, which is de-embedded before comparison with our model. The excellent match between our model and the 3-D field solver as well as measurement, as shown in Table I, validates the proposed Q-3-D model.

[2]Details of the dielectric layers and vertical dimensions of the metal layers are not given here. To deal with multi-layer dielectrics, we use effective dielectric constants as defined in [13].

C. General Non-Orthogonal Wires

In the general case of nonorthogonal crossover as described in Fig. 5(a), we note that area and edge are each increased by $1/\sin(\phi)$ for a rotation angle ϕ, leading to an increase of area capacitance and 2-D fringing capacitance. Fortunately, we find that $C_{wtw}(\phi)$ also assumes the same ϕ dependency. Thus $C_{cross}(\phi)$ and $W_{eff}(\phi)$ are generalized as

$$C_{cross}(\phi) = W_{eff}(\phi)C_{self} \tag{5}$$

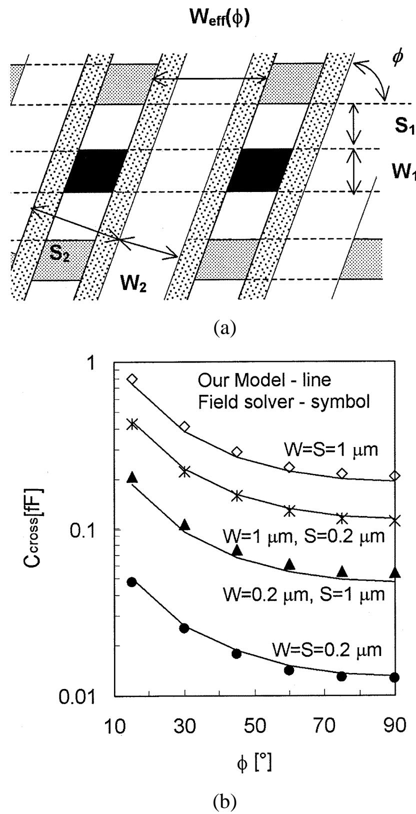


Fig. 5. (a) Schematic drawing of a general nonorthogonal crossover wire structure and (b) C_{cross} versus angle. In (b), where $S_1 = S_2 = 0.2$ μm, $T_1 = T_2 = 0.35$ μm, and $H_1 = H_2 = H_3 = 0.45$ μm, our model (line) and 3-D field solver (symbol) are compared.

where

$$W_{eff}(\phi) \equiv \frac{W_2}{\sin(\phi)} + \frac{W_1 C^{fr1}}{C_{self}\sin(\phi)} + \frac{C_{wtw}(90^\circ)}{C_{self}\sin(\phi)} = W_{eff}(90^\circ)\csc(\phi). \tag{6}$$

In Fig. 5(b), the generalized model shows excellent match with the 3-D field solver for a wide range of rotation angles.

With the generalized $W_{eff}(\phi)$, we can apply our Q-3-D model proposed in Section II-B to any general nonorthogonal wire structure. We extract the capacitance of a long wire loaded by two parallel neighbors and many crossover (and crossunder) wires with both orthogonal and diagonal routing, as shown in Fig. 6. Calculated W_{eff} of the crossover wire is given in Table II. As shown in Table II, W_{eff} is significantly larger than the physical width of the crossover wire (W). The results also show that inclusion of C_{wtw} in W_{eff} is critical for the structure. Capacitances extracted using our quasi-3-D method are compared with 3-D field-solver results, as shown in Table III. Excellent agreement between these results, with less than 3% error for both orthogonal and diagonal routings, further validates our generalized quasi-3-D model. In addition, either architecture yields virtually the same results. This is due to the fact that for a long wire, the number of crossover lines decreases by $\sin(\phi)$, which precisely offsets the increase in capacitance as given by (5) and (6). Furthermore, as shown in Table IV, if we use W instead of W_{eff} in the decomposition, substantial overestimation of C_{couple} and underestimation of C_{self} result. Such overestimation of C_{couple} will be highly undesirable for crosstalk analysis based on any capacitance model.

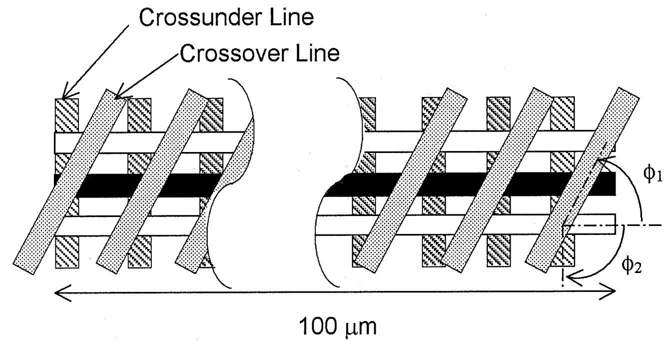


Fig. 6. Application structure to see parasitic capacitance of a long wire loaded by crossing lines with both orthogonal and diagonal routing. The angles of crossover and crossunder wires to the object wire are varied. Here we use $W = 0.4$ μm, $T = 0.35$ μm, and $H = 0.45$ μm for all metal layers. $S = 0.8$ μm for crossing lines and $S = 0.4$ μm for object layer are used.

TABLE II
COMPARISON BETWEEN PHYSICAL WIDTH (W) AND EFFECTIVE WIDTH (W_{eff} OR W'_{eff}) FOR ORTHOGONAL AND DIAGONAL ROUTING CASES SHOWN IN FIG. 6. W'_{eff} REPRESENTS EFFECTIVE WIDTH CALCULATED WITHOUT INCLUDING C_{wtw}

ϕ_1 \ Width[μm]	W	W_{eff}'	W_{eff}
90°	0.40	0.68	0.91
45°	0.40	0.96	1.27

TABLE III
TOTAL CAPACITANCE OF THE OBJECT LINE IN FIG. 6, EXTRACTED BY THE PROPOSED MODEL AND A FIELD SOLVER. NUMBERS IN PARENTHESIS ARE RELATIVE ERRORS

Routing \ C[fF]	Model	Field Solver
Orthogonal (ϕ_1=ϕ_1=90°)	19.7 (3%)	19.1
Diagonal I (ϕ_1=ϕ_2= 45°)	19.3 (2%)	19
Diagonal II (ϕ_1=90°, ϕ_2=45°)	19.5 (3%)	19

TABLE IV
CAPACITANCES OF THE OBJECT LINE IN FIG. 6 WITH $\phi_1 = \phi_2 = 90°$, EXTRACTED BY QUASI-3-D METHOD WITH TWO DIFFERENT DECOMPOSITION METHODS, EFFECTIVE WIDTH (W_{eff}) AND PHYSICAL WIDTH (W), ARE COMPARED WITH THOSE FROM FIELD SOLVER. NUMBERS IN PARENTHESIS ARE RELATIVE ERRORS

	Field Solver	Model using W_{eff}	Model using W
C_{couple} [fF]	9.0	9.2 (3%)	10.8 (20%)
C_{self} [fF]	10.1	10.4 (3%)	7.5 (-26%)
C_{total} [fF]	19.1	19.7 (3%)	18.3 (-4%)

III. AN EFFECTIVE LOOP INDUCTANCE MODEL

A typical high-speed on-chip interconnect configuration is shown in Fig. 7. At relatively low frequencies, each power grid provides a good current return path due to low resistance of the grid. As the frequency of the signal advances into the multi-GHz range, random signal lines start to participate in the return path. Eventually, at a sufficiently high frequency, virtually all the wires surrounding the high-speed signal line

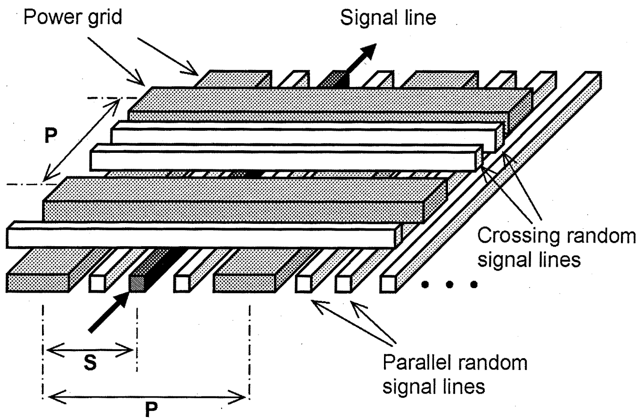


Fig. 7. Typical high-speed on-chip interconnects. Horizontal and vertical power grids are tied together through vias. P and S denote the pitch of power grid and the distance between signal line and the nearest power grid, respectively. Wires are assumed to be copper with a thickness of 0.35 μm each. Widths of signal line and power grid are assumed to be 1 μm and 4 μm, respectively.

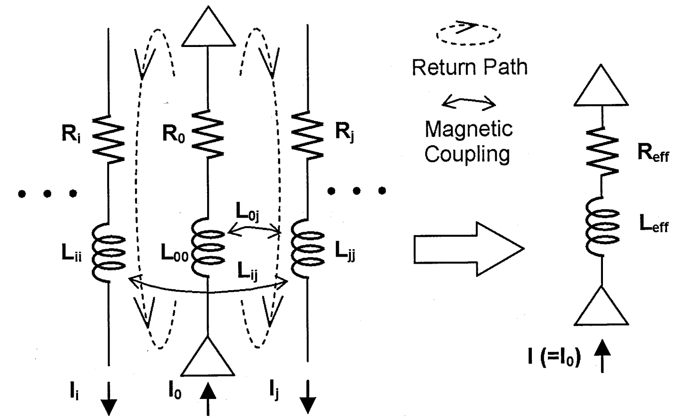


Fig. 8. Simplification of multiple return paths into a single signal line with effective resistance (R_{eff}) and effective inductance (L_{eff}). L_{ij} represents the partial inductance of ith line segment, induced by a current I_j flowing through jth line segment. I $(=I_0)$ represents the current flowing through the signal line, which is equal to the sum of all return currents I_j, $j > 0$.

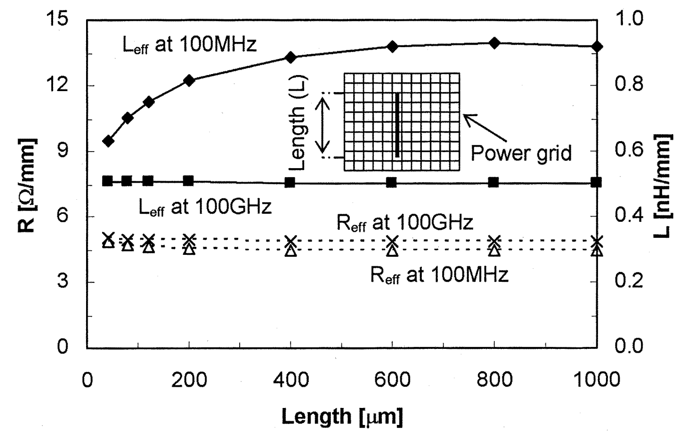


Fig. 9. R_{eff} and L_{eff} versus length of wire on power grid (see inset). $S = 3$ μm and $P = 40$ μm in Fig. 7 are assumed. In our FastHenry simulations, skin effect is not considered, in order to focus on proximity effect.

can function as possible return paths. Though Kleveland [7] demonstrated experimentally that random signal lines reduce the high-frequency inductance significantly, there has been no explicit modeling of this effect.

In this section, we propose an effective loop inductance model to account for the random-signal-line effect. Based on results from full-wave solver and S-parameter experiment, we propose an empirical high-frequency inductance model, which is extracted directly from the capacitance of the wire. We consider the return paths through the power grid and random signal lines separately in Sections III-A and III-B, and then combine their effects to arrive at a unified model in Section IV.

A. Compact Model Construction Using Effective Loop Inductance

As illustrated in Fig. 8, inductive interaction within every segment surrounding a signal line can be incorporated into an effective inductance, generating a single isolated RL model. The effective loop inductance (L_{eff}) and resistance (R_{eff}) in Fig. 8 can be derived [14], [15] using the equivalence of energy or power stored in the two systems, resulting

$$\frac{1}{2}\sum_i\sum_j L_{ij}I_iI_j \equiv \frac{1}{2}L_{eff}I^2 \tag{7}$$

$$\sum_k R_kI_k^2 \equiv R_{eff}I^2. \tag{8}$$

L_{ij} represents a partial inductance between segments i and j. I_i and R_i represent the current flowing through a segment i and the ohmic resistance of the segment, respectively. We use an analytical partial inductance model [16] for L_{ij} calculation, as outlined in Appendix B. In (7) and (8), we note that L_{eff} and R_{eff} are frequency-dependent because the return current (I_i) depends on frequency. Using these two equations, we obtain L_{eff} and R_{eff} in two frequency domains: low frequency (LF), where we assume that each return current is determined by only the resistances of all return paths, and medium frequency (MF), where only inductances are taken into account in determining the return current. Here the return current is through designated ground lines only. Finally, frequency dependency is implemented using the equivalent circuit as described in Section IV.

We investigate the linearity of L_{eff} and R_{eff} for a signal line on the power grid using FastHenry [17]. As shown in Fig. 9, L_{eff} and R_{eff} show excellent linearity, except at low frequencies for L_{eff}, where low-frequency inductance displays super-linearity because the return current spreads out as the length of wire increases. The linearity observed provides a sound basis for hierarchical model construction for a long wire by concatenating models of individual segments. Also we found that sufficient accuracy is achieved by considering only up to the second nearest power grid [18], making solutions of (7) and (8) manageable.

In Fig. 10, we compare our constructed model, for the structure shown in the inset with FastHenry. Our model shows excellent match except for a slight underestimation of inductance at low frequencies, which is caused by the super-linearity. Since low-frequency impedance is dominated by resistance, the underestimation has no significant effect on the total impedance of the signal line and on signal transfer characteristics [18].

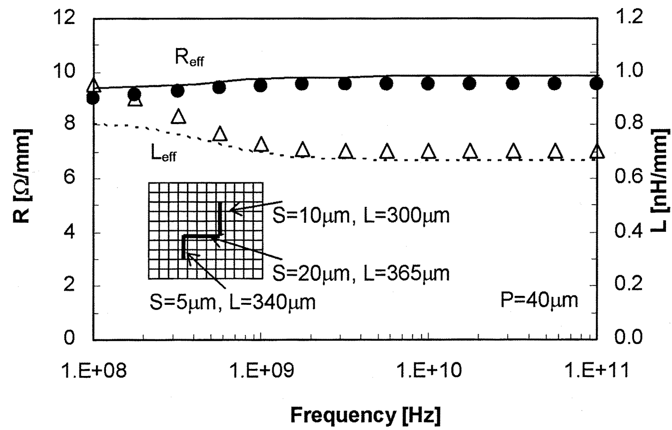


Fig. 10. L_{eff} extracted using our effective loop inductance model (line) is compared with FastHenry results (symbol) for a signal line on power grid as shown in inset. Here frequency dependency is modeled using the circuit shown in Fig. 13.

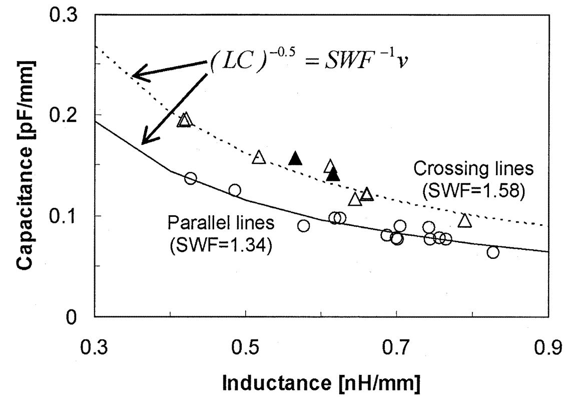


Fig. 11. Relationship between capacitance and inductance obtained from full-wave solver at 20.1 GHz for various capacitive coupling configurations. Lines represent the fitted slow-wave mode formulas given by (9), using simulation results (open triangles and circles). In full-wave solver simulations, low-k dielectrics with $k = 2.9$ are used for all structures. Solid triangles represent measured results for coplanar wave guide structures.

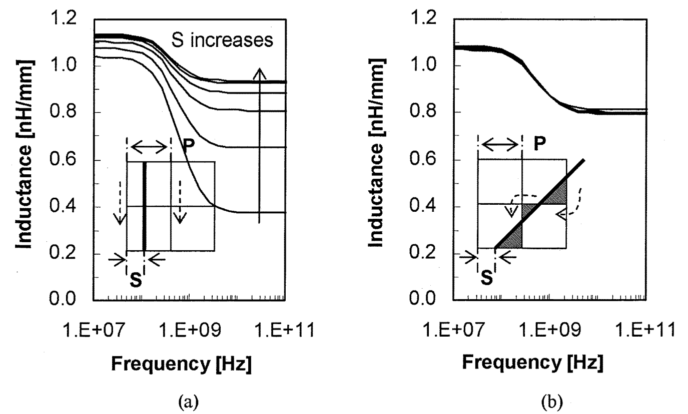


Fig. 12. Inductance versus frequency characteristics for different relative location of a wire to power grid. $S = 3, 5, 10, 15, 20, 25$ μm for each curve, while $P = 50$ μm. Diagonal wire (b) shows negligible change, while orthogonal wire (a) shows dramatic changes as S changes. Dashed arrows represent major return paths.

B. Random Signal Line Effect

We investigate this effect with a full-wave solver [19] for the structure shown in Fig. 7, where random signal lines are left floating [20]. Telegrapher's parameters, RLCG, are extracted from S-parameters obtained from simulation results. At high frequencies (HF), parallel random capacitive coupling can provide a pseudo ground line next to the signal line, inferring quasi TEM-mode wave propagation [20]. This hypothesis is supported by a close relationship between L and C in Fig. 11, extracted for the various structures with different configurations of random coupling lines. Based on lossless transmission line theory, the reciprocal of the LC product for TEM wave being the square of the phase velocity, our simulation data are fitted to a semi-empirical expression

$$(LC)^{-0.5} = SWF^{-1}\nu \tag{9}$$

where ν is the phase velocity in the medium and SWF is the dimensionless "slow-wave factor" used to characterize the deviation from ideal wave propagation along a lossless transmission line. In Fig. 11, crossing random coupling lines show a slightly slower wave-like propagation mode than parallel lines. It is well known that weaker coupling of electric and magnetic fields induce slower wave propagation [21]. Since the crossing lines cannot provide direct return path, the magnetic-field coupling between these wires and the object line is weaker than the electric-field coupling, thus weakening the coupling of the two fields, and slower propagation results. By introducing separate SWF's for parallel and crossing lines, which can be determined empirically for each technology, the high-frequency inductance in TEM-mode is extracted from the capacitance of the signal line. Here we note that the capacitance used in (9) to extract L_{HF} assumes floating random lines. The capacitance in (9) is calculated readily from a series combination of coupling capacitances, which are extracted as described in Section II, between the object signal line and ground line, through random lines. Since both parallel and crossing lines exist in a real chip, the final inductance value is calculated from a parallel combination of inductances due to parallel lines and crossing lines, respectively. By increasing extraction frequency from 20.1 GHz to 100 GHz, we find that the SWF changes by only 13%. Therefore, a single SWF (for parallel and crossing lines, respectively) can be used up to 100 GHz, which approaches unity at infinite frequency.

C. Non-Orthogonal Wires

Unlike orthogonal architecture, where horizontal and vertical wires are not magnetically coupled and can be treated separately, nonorthogonal architecture introduces increased complexity in inductance modeling due to magnetic coupling among nonorthogonal wires. We investigate inductive properties of a diagonal wire, which is a practical application of nonorthogonal architecture with a 45° crossing, using FastHenry [17]. A diagonal wire on a power grid [see the inset of Fig. 12(b)] shows linearity characteristics of the effective loop inductance similar to those for orthogonal wires as shown in Fig. 9.

One unique characteristic of the diagonal wire is illustrated in Fig. 12. For orthogonal wires, as demonstrated in Fig. 12(a), varying location of a signal line to power grid results in signif-

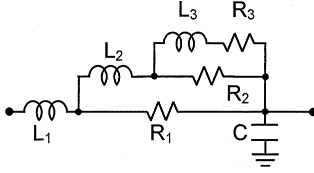


Fig. 13. Frequency-dependent RLC circuit model. The lumped element values are calculated using the (10).

icant changes in inductance, due to changes in magnetic flux between the signal line and return path. However, the diagonal wire inductance is insensitive to the relative location of the wires, as shown in Fig. 12(b). We attribute this to the fact that regardless of the signal line location, magnetic fluxes on opposite sides of the wire offset each other [see the inset of Fig. 12(b)], for this special case of 45° crossing. At high frequencies, similar SWF's are observed for diagonal crossing lines as orthogonal ones. Therefore any diagonal wire on the power grid can be modeled by an equivalent orthogonal wire on the power grid at some suitable separation S, independent of the location of the diagonal wire.

We verify our model by performing measurements on coplanar wave guide structures with orthogonal or diagonal random crossing lines, using a network analyzer, Agilent 8720 A. Measured values of L and C at 20.1 GHz are 0.566 nH/mm and 0.163 pF/mm for orthogonal wires and 0.615 nH/mm and 0.147 pF/mm for diagonal wires, respectively. These two data points are added to Fig. 11 and they further support the quasi-TEM mode description. Even without the inclusion of substrate effects in this study, this striking convergence provides the strongest evidence to date that at high frequencies, a system of interconnecting wires, regardless of its complexity, behaves much like that of single transmission line.

IV. Frequency-Dependent RLC Model

Capacitance model and inductance model developed in the previous sections are combined to yield a frequency-dependent RLC model as given in Fig. 13. We use parallel branches to model frequency dependency of R and L, as in Krauter [15]. The values of the lumped elements in the model can be calculated from the following six relationships with physical parameters extracted for any interconnect structure

$$\begin{aligned} R_{LF} &= R_1 \,\|R_2\|\, R_3; \\ L_{LF} &= L_1 + \left(\frac{R_1}{R_1 + R_2\,\|R_3}\right)^2 \left(L_2 + \left(\frac{R_2}{R_2+R_3}\right)^2 L_3\right); \\ R_{MF} &= R_1\,\|R_2\,; \qquad L_{MF} = L_1 + \left(\frac{R_1}{R_1+R_2}\right)^2 L_2; \\ R_{HF} &= R_1; \qquad L_{HF} = L_1. \end{aligned} \tag{10}$$

The low-frequency (LF) and moderate-frequency (MF) parameters, R_{LF}, L_{LF}, R_{MF}, and L_{MF} are extracted analytically from the configuration of the signal line and power grid as described in Section III-A, while high-frequency inductance (L_{HF}) is extracted from the capacitance for the configuration of random signal lines using (9). As described in Section III-B, the capacitance used in the extraction of L_{HF} is different from the

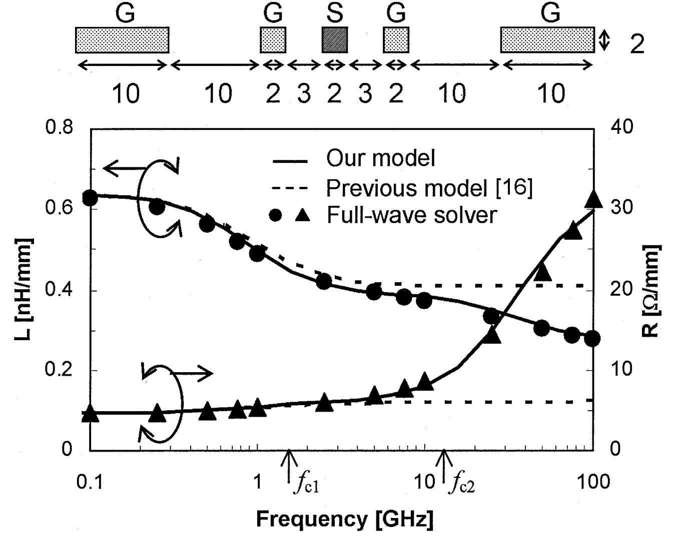


Fig. 14. Frequency-dependent resistance and inductance for a structure shown above. G and S denote ground and signal lines, respectively. Numbers in the structure represent dimensions of the structure in μm and random lines (both parallel and crossing) are not shown for simplicity.

lumped parasitic capacitance C in Fig. 13, which is extracted assuming grounded random signal lines as described in Section II. We use a modified skin-effect formula proposed by Kleveland [7] to extract high-frequency resistance (R_{HF}). With the proposed RLC model, the frequency behaviors of L_{eff} and R_{eff} show three distinct regions, namely, low, medium, and high, where different return paths dominate. Since the return path is determined by a competition between its inductive and resistive impedances, two crossover frequencies, f_{c1} and f_{c2}, which separate the three regions, are defined as

$$f_{c1} = \frac{R_{MF}}{2\pi L_{LF}}, \qquad f_{c2} = \frac{R_{HF}}{2\pi L_{MF}}. \tag{11}$$

Below f_{c1}, the bulk of the current returns through the least-resistive path. Between f_{c1} and f_{c2}, we assume that current returns through the least-inductive path provided by designated ground lines. Above f_{c2}, current returns through the least inductive path provided by random signal lines through capacitive coupling as well as by designated ground lines.

In Fig. 14, our model is compared with Krauter's model [15] as well as with a full-wave solver. Our model shows excellent match for a wide range of frequencies, from 100 MHz to 100 GHz, while Krauter's model significantly overestimates high-frequency inductance and considerably underestimates high-frequency resistance. For this comparison, f_{c1} and f_{c2} are found to be 1.5 GHz and 13.5 GHz, respectively.

Being based on closed-form equations for inductance and capacitance extraction, our model provides high computational efficiency for full-chip-level applications.For the structures shown in Figs. 4 and 6, our capacitance model requires orders of magnitude less computational time than a field solver, even if we use a solver incorporating the random-walk method[3] instead of a conventional (and slower) solver employing the multipole-accelerated boundary integral method. Thus our hierarchical and an-

[3]"QuickCap," from Random Logic Corporation.

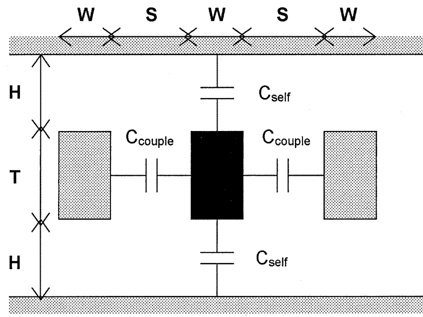


Fig. 15. Parallel 2-D wires between two ground planes with geometrical parameters and related capacitance components. Black line in the center is the object line, which is being modeled.

alytical methodology demonstrated for inductance model construction forms the basis for full-chip-level applications.

V. CONCLUSION

Aiming for full-chip-level applications, we propose a unified compact RLC model for high-speed on-chip interconnects. A unified quasi-3-D capacitance model for general nonorthogonal wires based on a novel concept of effective width (W_{eff}) is proposed. A new analytical wall-to-wall model as well as an analytical 2-D model is included in the proposed model, and confirmed to provide high accuracy for deep sub-micron technology, by extensive comparisons with field solver and measurement results for various test structures.

A first-ever effective loop inductance model for practical on-chip interconnects with random capacitive coupling is proposed in this paper. The validity of the effective loop inductance and hierarchical model construction methodology are demonstrated. The effect of random signal lines on the on-chip inductance is quantitatively investigated, using an S-parameter-based methodology and a full-wave solver. In particular, quasi TEM-wave-like propagation mode is observed above 10 GHz, revealing a unique empirical relationship between capacitance and inductance of the signal line. This relationship is believed to be valid for all interconnects at high frequencies.

By combining the quasi-3-D capacitance model and effective loop inductance model, we have successfully created a scheme whereby compact modeling and parameter extraction for high-speed on-chip interconnects can be readily conducted.

APPENDIX A
CAPACITANCE FORMULAS

For structure and notations of the geometrical parameters, refer to Fig. 15 for 2-D model and Fig. 1 for 3-D model. In the following equations, subscript *self* or *couple* means self or coupling component of the line capacitance and superscript a or fr means area or fringing component of the line capacitance. 2-D capacitance model is modified from Chern's model [9] and 3-D model is solely our contribution.

Although Chern's 2-D model generally provides accurate results for most cases, it showed relatively poor results for thick dielectrics [13], which are important in today's technology with multi-metal layer. We optimize empirical parameters separately for area and fringing components. Furthermore a finite constant term is added in the fringing capacitance formula to account for an asymptotic contribution due to the edge of each plate, in the zero limit width and thickness limit. This constant term results in a more physical [22] and accurate model. Our 2-D model shows an average error of 1.6% and a maximum error of 3.5%, while Chern's model shows 4.9% and 17.9%, respectively, for the ranges: $0.29 \leq W/T$, $S/T \leq 14.3$, $0.22 \leq W/H$, $S/H \leq 11.1$, $0.71 \leq H/T \leq 11.43$, all in μm units [13]. Our 3-D wall-to-wall model is confirmed for the ranges: $0.1 \leq W, S \leq 5, 0.1 \leq T \leq 2, 0.25 \leq H \leq 4$, with an average error of 3% and a maximum error of 10%.

1) Two-dimensional capacitances (scaled by the dielectric permittivity):

$$C_{couple}^{a}/\varepsilon = \frac{T}{S}\left(1 - 1.5e^{T/2.5S}e^{-(H/0.31S)} + 1.5e^{-(H/0.08S)} - 0.13e^{-(T/1.3S)}\right) \quad (12)$$

$$C_{couple}^{fr}/\varepsilon = \left(\frac{H}{S}\right)^{0.2}\left(1.53 - 0.98e^{-(W/0.35H)}\right) \cdot e^{-(S/0.65H)} + 0.01 \quad (13)$$

$$C_{self}^{a}/\varepsilon = \frac{W}{H} \quad (14)$$

$$C_{self}^{fr}/\varepsilon = \left(1.05 + 0.63e^{-(T/S)} - e^{-(S/1.2H)}\right) \cdot \left(\frac{S}{S+2H}\right)^{0.05}\left(\frac{T}{H}\right)^{0.25} + 0.063. \quad (15)$$

2) Three-dimensional wall-to-wall capacitance (scaled by the dielectric permittivity):

$$\frac{C_{wtw}}{\varepsilon} = 20\left[0.2 + 0.8\exp\left(\frac{-0.6T_1}{S_1}\right) + 0.8\exp\left(\frac{-0.6T_2}{S_2}\right) + 0.45\exp\left(-0.45\frac{W_1}{H_1}\right) + 0.45\exp\left(-0.45\frac{W_2}{H_3}\right)\right] \cdot \left[\frac{d_{eff}}{(d_{eff}+4H_2)}\right]^{2.4} H_2, \quad (16)$$

where

$$\frac{1}{d_{eff}} = 0.25\left[\frac{1}{S_1} + \frac{1}{S_2} + \frac{2}{(T_1+H_1)} + \frac{2}{(T_2+H_3)}\right]$$

represents shielding effect from the neighbors surrounding the crossover.

APPENDIX B
INDUCTANCE FORMULAS

We use Grover's formulas [16], which are simple yet accurate enough to extract the partial inductance L_{ij} of on-chip interconnect, for which inductive effect becomes significant. Note that all Ls are given in units of nanohenry, and l, W, and T are length, width, and thickness of the wire in units of micrometer.

1) Self inductance L_{ii} of the ith wire is given by

$$L_{ii} = 0.0002l\left[\ln\left(\frac{2l}{W+T}\right) + 0.5 - \ln\lambda\right], \quad (17)$$

where $\ln \lambda$ is a slowly varying function of the ratio W/T, ranging from 0 to 0.002 49. For the case of $l > (W+T)$, $\ln \lambda$ is negligible with less than 1% error.

2) Mutual inductance L_{ij} between parallel wires i and j of equal length

$$L_{ij} = 0.0002l \left[\ln\left(\frac{l}{d} + \sqrt{1+\frac{l^2}{d^2}} \right) - \sqrt{1+\frac{l^2}{d^2}} + \frac{d}{l} \right], \tag{18}$$

where d represents the geometrical mean distance (GMD) between the two wires, which depends on width (W) and thickness (T) of the wires and space (S) between the wires. In the special case of $l \gg d$ or $W \cong T$, we can use a simple arithmetic mean distance (AMD) instead of GMD without any substantial error. Since no analytic form of GMD is available for the general case, however, a table look-up method [16] or a more complicated analytic [14] can be used.

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