On-Chip Interconnect Conductor Materials for End-of-Roadmap Technology Nodes

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***Abstract*—A comprehensive review of challenges and potential solutions associated with the impact of downscaling of integrated circuit (IC) feature sizes on on-chip interconnect materials is presented. The adoption of Moore's Law has led to developments and manufacturing of transistors with nanoscale dimensions, faster switching speeds, lower power consumption, and lower costs in recent generations of IC technology nodes. However, shrinking dimensions of wires connecting transistors have resulted in degradations in both performance and reliability, which in turn limit chip speed and lifetime. Therefore, to sustain the continuous downward scaling, alternative interconnect conductor materials to replace copper (Cu) and tungsten (W) must be explored to meet and overcome these challenges.**

***Index Terms*—Carbon nanotube, cobalt, contact, graphene, interconnect, low-*k*, resistance, resistivity, ruthenium, silicides.**

I. Introduction

FOR the past five decades, there have been significant advancements in computer technologies due to an enormous surge in computing power and reduction in computer form factors. This has enabled rapid developments of various computer-based consumer products such as desktops, laptops, tablets, smartphones, navigation systems, smart home appliances, and self-driven cars. Integrated circuit (IC) or chip technology, which allows the manufacture of the entire circuit or system on a monolithic silicon or other semiconductor substrates, is the primary engine driving the form factor reduction. For every generation of products, dimensions of components on an IC are scaled downwards, enabling increased functionality and data storage per unit area [1]. The signals processed by transistors and their accompanying power are transported between transistors via on-chip interconnect conductors. In current digital circuits, transistors are usually made from silicon and interconnect conductors from copper (Cu) and tungsten (W) [1]. In the early years of chip manufacturing, component dimensions were downscaled continuously, resulting in approximately doubling the number of transistors on-chip every year, as observed by Gordon Moore in 1965 [2]. He later revised this empirical trend to doubling the number of transistors on-chip every two years, famously known as Moore's law [3]. This non-science-based projection has been adopted throughout the IC industry since and its realization was made technologically possible by advancements in photolithography, which allows downscaling of fabricated chip components to continue to the present [1]. Reducing transistor dimensions results in lower operating voltages, increased switching speeds, and less power consumption. Such performance improvements in turn yield orders of magnitude increase in switching speed or clock frequency of microprocessors from the initial generation of Intel 4004 (750 kHz) [4] to Pentium-IV (3.8 GHz) [5] and now sixth generation Core i7 which has four data processing cores each with clock speed 4.2 GHz, built using Intel's 14 nm process technology [6]. AMD's FX processor built using 32 nm silicon-on-insulator (SOI) technology has a clock speed of 5 GHz and can be overdriven up to 8.6 GHz, the highest ever for consumer applications [7]. However, downscaling of interconnect dimensions raises the conductor resistance as well as inter-metal capacitance, thus hampering chip performance [8]. Further, as interconnect linewidths are reduced, the current density increases, leading to material breakdown along the conducting path and circuit failure. Therefore, alternative interconnect conductors are needed that can withstand aggressive performance and reliability constraints posed by advanced semiconductor technology.

As a review of the state-of-the-art of on-chip interconnects, the following section of this paper addresses the impact of downscaling on performance and reliability of existing interconnects and the engineering solutions to meet the resulting challenges. Section III describes the advantages and challenges associated with potential materials to replace Cu and W. Studies of a promising candidate for next-generation interconnects, carbon nanotube, are summarized in Section IV of this review paper.

II. Moore's Law and its Impact on Interconnects

As mentioned above, Moore's law served as the guide to photolithography-driven downward scaling of semiconductor components. Every 24 months, a new IC technology node has been brought to high-volume production. Every new node has components printed on a monolithic silicon substrate with dimensions scaled by $\sim 0.7\times$ the previous node. Components on a chip can be classified into three categories depending on the stage in the manufacturing process. The first is Front-End-of-Line (FEOL) for transistor fabrication. Then comes the

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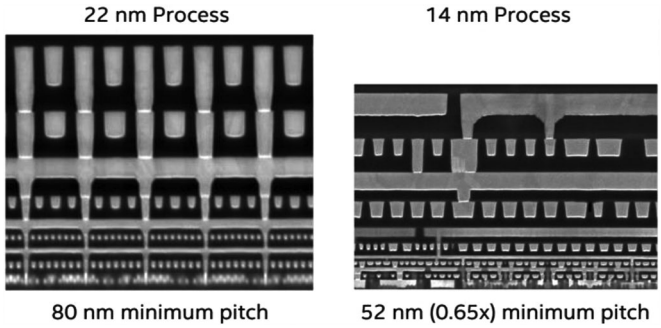

Fig. 1. Cross-sectional SEM images of chips from Intel's 22 nm and 14 nm processes, showing downscaling of components by 0.65 [9].

Middle-of-Line (MOL) which includes contacts to source/drain regions of transistors and the first metal level consisting of W interconnects. The final category is the Back-End-of-Line (BEOL) for the upper levels of Cu metallization [1]. Fig. 1 shows cross-sectional scanning electron microscope (SEM) images of a chip fabricated by Intel using technologies from two recent nodes [9].

The IC building block is metal-oxide-semiconductor field-effect transistor (MOSFET), which can be used for both analog and digital applications. For the latter, it functions as a voltage-controlled switch (ON/OFF) through suitable combinations of gate and source/drain biases. With downscaling of transistor dimensions, features such as gate capacitance are reduced [1]. This allows the transistor to function at a voltage lower than that for the previous node while storing less charge. Lower operating voltage and shorter charge-discharge cycle result in transistors with less power consumption and faster switching speed. Thus transistor performance is enhanced by downscaling its dimensions [1]. However, leakage current due to reduced gate dielectrics thickness and control of gate over channel present challenges. To mitigate such challenges, high-*k* gate dielectrics have been deployed [12] and new device structures such as FinFET and Gate-all-around were introduced [13]. These new technologies are prevalent in advanced technology nodes [14].

A Cu interconnects structure consists of the following components: barrier layer to prevent Cu diffusion into the surrounding dielectric, nucleation layer on the barrier material to enable metal film growth, and bulk metal fill [11]. As interconnect dimensions are scaled, the thickness and volume of each layer are reduced. For Cu and W interconnects, downscaling interconnect dimensions causes electrical resistivity of Cu and W to rise significantly in the sub-50 nm regime [11]. This is a result of increased electron scattering at metal grain boundaries and at surface/interfaces. A schematic of such scattering phenomena in an interconnect structure is shown in Fig. 2(a) with measured resistivity data in Fig. 2(b).

Parameters contributing to the total resistance of an interconnect consist of electrical resistivity of conductor filling it, contact resistance, and geometry [11]. With continued downscaling of dimensions, besides surge in resistivity, contact resistance also increases as the contact area is reduced. Thus the resulting increase in overall resistance degrades the interconnect performance. Another factor governing interconnect performance is inter-metal capacitance, which depends on geometry

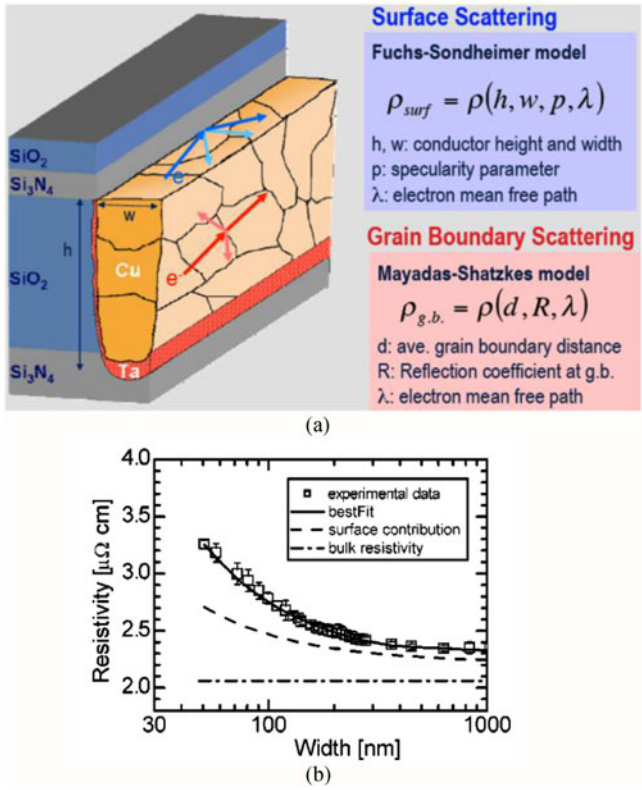

Fig. 2. (a) Schematic of electron scattering at grain boundaries and surfaces inside a copper trench structure [10]. (b) Corresponding measured resistivity trend for Cu wires down to 50 nm linewidth [11].

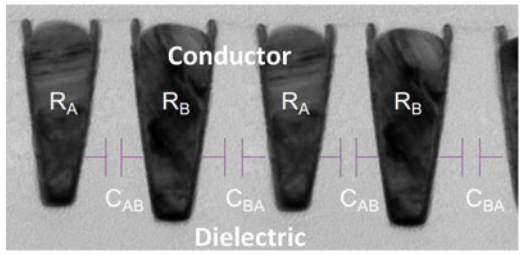

Fig. 3. Resistance and capacitance components in an interconnect structure [1].

and dielectric constant *k* of the surrounding insulating material. The resistance and capacitance components in an interconnect structure are indicated in the cross-sectional TEM image shown in Fig. 3.

In general, performance of interconnects is measured by the time taken by an electric signal to propagate through the network of lines and vias. This delay in signal propagation is expressed as $\tau = RC$, where *R* is resistance and *C* the capacitance of the entire interconnect system. As downscaling results in increase in *R*, the resulting increase in delay is compensated by employing a dielectric material with a lower *k* which then reduces *C*. Intel's recent release of 14 nm process technology shows that air gaps were employed in the dielectric network to further reduce the effective *k* and lower the capacitance [9]. The requirements for effective dielectric constant k_{eff} for subsequent nodes are given in Fig. 4.

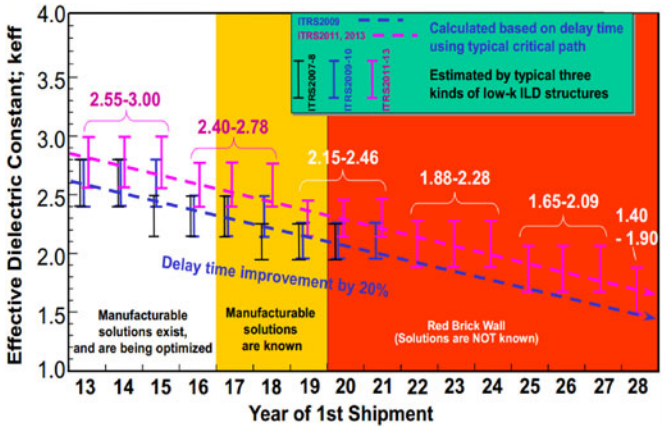

Fig. 4. Projected effective dielectric constant for interconnect system to manage propagation delay [1].

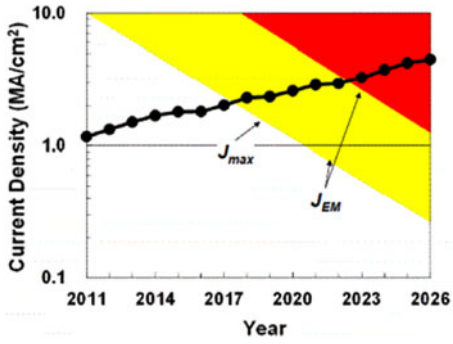

Fig. 5. Projected maximum current density J_{max} through interconnects for future technology generations. The yellow and red shaded regions indicate EM and post-EM regimes, respectively. While I_{max} through the interconnect is scaled downwards for each generation, J_{max} increases due to continuous reduction of interconnect cross-sectional area [1].

In 1997, Sun [8] reported a detailed analysis on the effect of scaling on transistor (gate), interconnect, and unit circuit (gate + interconnect) performance, in which two interconnect systems, Al/SiO_2 and Cu/low-*k*, were compared for linewidths from 0.65 to 0.09 μm. With continued downscaling, the performance of the Al/SiO_2 system degraded drastically in this node range. On the other hand, the corresponding increase in delay for the Cu/low-*k* material system was much less, making it a viable substitute for the Al/SiO_2 system in sub-100 nm nodes. However, at 180 nm node, even the Cu/low-*k* system's delay surpassed that from the gate and the total delay decreases up to the point where interconnect and gate delays are comparable, beyond which the total delay of the unit begins to increase. Thus, according to Sun's projection [8], the performance of a circuit would be dominated by interconnects in the sub-180 nm regime and the impact would be more acute in the sub-30 nm nodes as the surge in interconnect delay continues, due largely to increase in conductor resistance [1]. Therefore, alternative conductor materials would be needed to replace Cu and W at sub-30 nm technology nodes to mitigate this resistance increase.

Aside from performance, the other critical metric for an interconnect system is its reliability, which is the extent to which an interconnect can maintain charge flow through it without degradation in performance or worse, such as material breakdown. Downscaling of interconnect dimensions at each node results in a reduction of cross-sectional area and the maximum current through it before the conductor breaks down. At the same time, the operating current density J, in A/cm^2, in a circuit increases with downscaling [15]. Once the current density approaches the current-carrying capacity for a conductor material, the electric field associated with the moving electrons is sufficiently large to displace the atoms from their lattice sites along the current path. This phenomenon is known as electromigration (EM). If the conductor operates at or near its EM limit frequently, void formations along the current path can result, leading to an open circuit and chip failure. The maximum current density projected for interconnects in future nodes J_{max} is given in Fig. 5 [15], which shows $J_{max} \geq 2$ MA/cm^2 from 2014 on. Cu and W possess bulk maximum current-carrying capacities of 2 MA/cm^2 and 1 MA/cm^2, respectively, and clearly cannot meet such current density requirements [1]. Therefore, materials engineering approaches for extending the electromigration limit were introduced to enhance the reliability of conventional materials [1].

One such approach is to consider the Blech length (L_B) in designing interconnects, defined as the maximum length of conductor at which the internal mechanical stress can offset electromigration [15]. If the (J $\times$ conductor length) product is less than the critical product ($J_C \times L_B$), where J_C is the critical current density for EM failure [16], electromigration does not occur. Therefore, lengths of Cu interconnects are designed in such a way that the (J_{max} $\times$ conductor length) product does not exceed the critical value. The critical product is dependent on thermomechanical properties of the interconnect system. For example, Cu/SiO_2 has a higher critical product than Cu/low-*k* porous film used at advanced nodes to reduce the interconnect capacitance [17]. The critical product for the latter is 2500 A/cm, giving values of $L_B = 25 \sim 8.3\,\mu$m for $J_C = 1 \sim 3$ MA/cm^2 [17]. Further increase in the porosity of dielectric film will reduce the critical product, limit the Blech length, and result in electromigration for current densities operating in the range above 2 MA/cm^2 for future nodes, as illustrated in Fig. 5. Thus the tradeoff between lowering interconnect capacitance and avoiding EM must be carefully managed.

Another approach is adding a capping layer on Cu to prevent mass transport out of the Cu bulk using the adhesive force between Cu and capping layer [18]. The selection criterion is minimum added resistance to interconnect with an extended lifetime. An analysis of the EM lifetime versus resistance increase behavior was used to identify capping materials that yield higher slope, having enhanced EM lifetime with minimum impact on resistance [1]. The results showed that CuSiN with Ti as barrier metal (BM) and CoWP were the most suitable materials for capping Cu interconnects [1]. Combining Blech length consideration and capping layer in designing interconnects, the current-carrying capacity of Cu can be extended to 3 MA/cm^2 [1]. Fig. 5 shows that the interconnect current density requirements are approaching 5 MA/cm^2 for the most advanced nodes. Therefore, in order to continue the downward scaling trend and

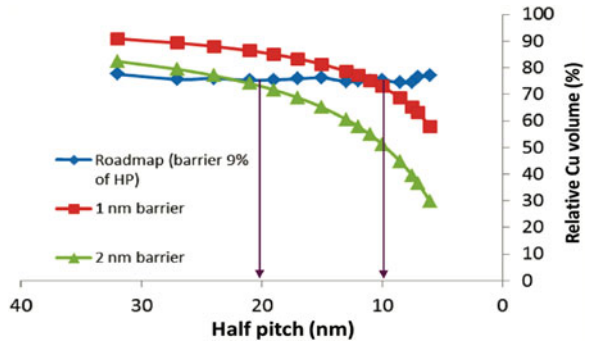

Fig. 6. Percentage of Cu volume in trench structure versus its half pitch (HP) [20].

meet such J_{max} requirements, alternative conductor materials which can match the performance of Cu and W while exceeding the reliability requirements are needed.

III. Potential Replacement Interconnect Conductors

With reduced interconnect dimensions at sub-30 nm nodes, the resistivities of Cu and W increase significantly from their respective bulk values of 1.7 $\mu\Omega$·cm and 11 $\mu\Omega$·cm due to enhanced electron scattering at conductor surfaces and grain boundaries [11]. Hence, to mitigate the resulting performance degradation, alternative conductors with smaller resistivities at such dimensions are needed. One criterion for evaluating potential replacement materials is lesser resistance degradation than Cu and W with downscaling [1]. Another is that high-resistance barrier and seed layers are not required [19], as these layers can reduce the relative Cu volume by as much as 70% as shown in Fig. 6, resulting in further performance degradation.

The evaluation of potential replacement conductors is being pursued using one of three approaches, as described in [1] and [19]. In the first approach, materials with smaller electron mean free path than those of Cu and W such as silicides (in particular Ni silicides) have been evaluated extensively. The monosilicide phase, NiSi, has been demonstrated to preserve its bulk resistivities ($\sim$10 $\mu\Omega$·cm) for single crystal nanowires (SCNW) with diameters down to 58 nm, attributable to NiSi having significantly smaller electron mean free path ($\sim$5 nm) compared to Cu and W [21]. SCNW using other phases of Ni silicides such as $NiSi_2$ and Ni_2Si exhibited resistivities of 30 $\mu\Omega$·cm and 21 $\mu\Omega$·cm for diameters down to 40 nm [22] and 34 nm [23], respectively, both preserving their bulk resistivities. Thus, the monosilicide phase seems to have the lowest resistivities for the dimensions of interest. By virtue of their single-crystalline nature, current-carrying capacity of NiSi SCNW is in the range of 100 MA/cm^2 [22]. Thus single-crystalline NiSi is a potential candidate as an interconnect via material. The experiments reported so far consists of either NiSi thin films or test structures consisting of NiSi nanowires fabricated by annealing of Ni on self-assembled Si nanowires [22]. A process to selectively deposit Ni silicide in an integrated interconnect or via structure with the desired phase has yet to be demonstrated but continues to be investigated [1].

The second approach is to evaluate materials having significantly longer electron mean free path than Cu and W. Single-walled and multi-walled CNTs (MWCNTs) are known to exhibit electron mean free paths in the micrometer range. MWCNTs have been studied extensively during the last decade as a potential on-chip interconnect material, pioneered by Graham [24] who reported findings on the first 30 nm CNT via. Subsequently, various academic and industrial research groups have focused on different aspects of realizing CNT vias. Nihei [25] focused on developing a process of integrating CNT vias that is compatible with BEOL thermal budget of 400$\sim$450 °C. Their most recent report demonstrated a CNT via with 70 nm width and aspect ratio of $\sim$1, yielding a resistance of 11 kΩ [26]. Vollebregt [27] also focused on lowering the CNT growth temperature to as low as 350 °C. However, the feature sizes of interconnects reported were in the 1-3 μm range, much larger than those in advanced technology nodes. Van der Veen [28] characterized CNT vias with 150 nm width and Cu contact integration. Chiodarelli [29] focused on increasing the packing density of CNT in a via by employing an AlCu alloy underlayer, which enhanced Fe catalyst dewetting to increase CNT packing density in a via. This approach resulted in more CNT shells as conducting paths and could potentially yield lower via resistance. However, their low-temperature CNT growth resulted in via resistance in the 10 kΩ range. Growing CNTs at low temperature introduces defects which in turn reduces electron mean free path and increases resistance. Therefore, for BEOL-compatible process CNT via resistance remains significantly higher than its Cu and W counterparts. Nevertheless, CNTs exhibit high mechanical strength in their structure due to sp^2 C-C bonding which makes them resistant to electromigration. Current-carrying capacities reported for CNT vias generally range from 100 to 1000 MA/cm^2 [30]. Such attractive reliability makes CNT a contender to replace Cu and W, especially in vias, if the CNT via resistance can be reduced to approach its Cu and W counterparts. To achieve better CNT via performance is indeed a daunting challenge, which at the very least requires lowering contact resistance and via resistance by optimizing CNT growth and contact metallization processes.

The third approach to identify suitable materials to replace Cu was reported by van der Veen in 2015 [19]. Cu and W interconnects require barrier and liner layers in the interconnect structure to provide diffusion barrier and adhesion, respectively. Addition of these resistive layers reduces the total volume available for low-resistivity Cu and W. Therefore, if an alternative conductor can be integrated with the surrounding low-k dielectric without the need for any barrier and liner, it can yield lower via resistance than Cu at sub-20 nm linewidths [19]. Electroless deposited Co in a via structure was demonstrated to possess such characteristics [19]. As shown in Fig. 7(a), Co outperforms Cu with barrier for widths below 15 nm. The delay due to barrierless Co interconnects with airgap is $\sim$67% lower than that from Cu interconnects, and even lower than gate delay at 5 nm node, as shown in Fig. 7(b). Such advances have extended the interconnect-dominated regime to well in the sub- 10 nm nodes, from 180 nm projected in 1997 [8], thus underscoring the significant improvements in interconnect technology since then.

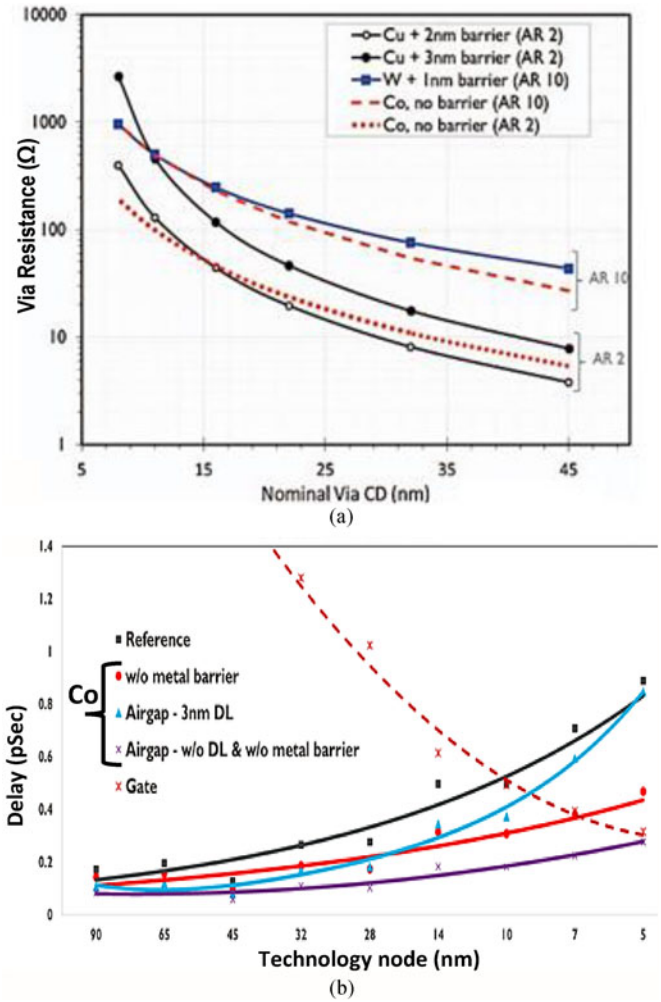

Fig. 7. (a) Comparison of Cu, W, and Co resistances for different linewidths [19]. (b) Comparison of delays from various interconnect configurations with gate delay [20]. Note: Reference is for Cu/Low-k system with barrier and seed layers.

Compared to nanocarbons, Co is more compatible with conventional silicon IC processes, as it can be deposited using chemical vapor deposition (CVD) with organometallic or metal-halide precursors [19]. Kim [31] reported a resistivity of 22 $\mu\Omega$-cm for 10 nm thick CVD Co film using organometallic precursor. The current-carrying capacity of Co is similar to that of Cu ($1 \sim 3$ MA/cm^2) [19]. Thus, reliability challenges will remain for Co interconnects in future nodes. Very recently, similar results for Ru interconnects were reported [32]. The properties of candidates to replace Cu and W in interconnect vias are summarized in Table I.

The reported via dimensions, material resistivity, via resistance, contact resistance, and via current-carrying capacity for each material are given in Table 1. While the performance and IC process compatibility of Co and Ru as interconnect via materials are superior to what are currently known about CNTs, the incomparably high current capacity of CNT keeps it viable as a leading candidate to replace Cu and W in sub-10 nm technology nodes. Such appealing reliability will continue to drive further research to improve the CNT via performance and to narrow the gap in IC process compatibility.

TABLE I
PROPERTIES OF CANDIDATE MATERIALS FOR INTERCONNECT VIAS AND COMPARISON WITH CU AND W

Material	Dimensions (Width × Length)	Resistance (kΩ)	Resistivity ($\mu\Omega$-cm)	Contact Resistance (kΩ)	Via Current Capacity (MA·cm^2)
NiSi nanowire [21]	58 nm × 2.9 μm	0.066	10.8	NA	100
Co [19]	9 nm × 18 nm	0.11	22	NA	1∼2
Ru [32]	20 nm × 1 μm	0.200	18	NA	6.5
Ag Nanowire [33]	28 nm × 1.4 μm	1.3	42.7	0.365	10
CNT [24]	30 nm × 150 nm	7.8	NA	NA	400
Multi-layer graphene [34]	250 nm × 5 μm	3.8	10	1	500
Cu [35]	30 nm × 130 nm	0.024	7	15	2
W [36]	30 nm × 130 nm	0.060	38	5	1

IV. STATE OF CNT INTERCONNECTS

CNT has been extensively studied as a potential replacement interconnect material since the turn of the millennium. Its performance and reliability in both horizontal and vertical configurations have been investigated. In the vertical configuration, integrating an aligned array of CNTs in an on-chip patterned array of vias and growing a CNT bundle at metal contacts have been achieved [27]. On the other hand, fashioning horizontal CNTs at a pre-defined location on a substrate while controlling the packing density posed additional challenges [37]. Nonetheless, on-chip CNT FETs and high-density horizontal CNT interconnects were successfully integrated by multiple transfers of pre-grown CNTs onto the final substrate [38]. Recently, an 8-bit CNT-based computer was demonstrated using such technique [39], while in most CNT reports on horizontal interconnects, drop-casting CNTs on pre-patterned test-structures was carried out [40], [41]. Table II summarizes the current state of horizontal CNT interconnects based on electrical measurements from DC to radio-frequency (RF), the given value for the latter at maximum frequency. The decrease in resistance from DC to RF evident in most cases is attributed to improvement in contact impedance due to its low capacitive component at the CNT-metal interface at high frequency, which serves as an electrical shunt at the contact. This frequency dependence results in significant variations of interconnect performance at different frequencies. Therefore, it is desirable to improve the contact impedance by depositing a high-purity material at the CNT contacts. Contacts with deposited Pt and W have been shown to reduce the overall impedance of the interconnect structure, with negligible frequency dependence and vanishingly small reactive component [40], [41].

Vertically aligned CNTs have been integrated in patterned vias with widths ranging from microns to sub-100 nm. In order to evaluate CNT vias with relevant linewidths and at BEOL-

TABLE II
SUMMARY OF CURRENT STATE OF HORIZONTAL CNT INTERCONNECTS

CNT type	Electrical Measurement	Length/ Diameter	R_{Total} (DC & RF) kΩ	L_{CNT}	C_{CNT} (fF)	Contact metal
MWCNT [40]	0-50 GHz	4 μm/150 nm	7.1/6.5	NA	NA	W
SWCNT [42]	0-10 GHz	25 μm/2 nm	150/150	NA	NA	Cr/Au
SWCNT bundle [43]	0-50 GHz	5 μm/1.1 nm	0.8/0.75	37 pH	27	NA
MWCNT [44]	0 - 50 GHz	5 μm/25 nm	7.8/0.28	215-0.02 μH	3.5-0.9	Nb
MWCNT [45]	0-110 GHz	8 μm/18 nm	15/0.2	18-0.1 nH	10 – 0.1	Au
MWCNT [38]	0-15 GHz	5 μm/70 nm	20/3	NA	1.5	Au
SWCNT [46]	0-7 GHz	1 μm/NA	20/13	70 nH	17	Au/Pd
MWCNT [47]	0-50 GHz	2 μm/70 nm	11/8	NA	0.1	Pt
MWCNT [48]	0-24 GHz	5 μm/30 nm	400/1	NA	1.4	EBID-C

TABLE III
SUMMARY OF CURRENT STATE OF CNT VIA INTERCONNECTS

Via (in nm)	CNT growth temper-ature (°C)	CNT Areal Density (#/cm^2)	Via Resistance (kΩ)	CNT resistivity (mΩ-cm)	Contact resistance (kΩ)	Current Capacity (MA/cm^2)
40/80 [49]	700	10^{12}	6.1	1.8	2.84	330
30/150 [24]	700	1.5×10^{11}	7.8	0.15	NA	400
70/80 [26]	450	3×10^{11}	11	NA	NA	100
300/450 [29]	470	2×10^{11}	8	3.7	1.16	NA
150/360 [50]	540	$\sim 10^{11}$	7	5.1	1.8	NA
1000/1000 [27]	350	10^{10}	0.159	110	NA	NA

compatible temperatures [27], the experimental focus has been on growing CNTs at temperatures less than 450 °C, as indicated in Table III, which summarizes reported results for CNT vias. Growth at temperatures below 700 °C results in CNTs with high defect densities [27], while good-quality CNTs grown in 30 nm vias at 700 °C were demonstrated [24]. The most recent resistivity and contact resistance of CNT vias with 40 nm linewidth were 1.8 mΩ·cm and 2.84 kΩ, respectively. These values are still two orders of magnitude higher than their conventional Cu and W counterparts.

V. CONCLUSION

The performance and reliability challenges associated with downscaling of Cu and W interconnects have been discussed in light of the demands and constraints mandated by technology roadmap. The adverse effects on performance can be mitigated to some extent by tuning the dielectric porosity and using conductors that do not require barrier materials. However, in sub-10 nm nodes, no conventional metals can meet the maximum current density requirement of 5×10^6 A/cm^2. With current-carrying capacities far exceeding such required value, CNT remains a viable potential replacement for Cu and W. However, there are challenges associated with processing temperature, high resistivity, defect control and contact resistance that need to be overcome to realize such potential.

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