Structural and Electrical Characterization of Carbon Nanofibers for Interconnect Via Applications

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***Abstract*—We present temperature-dependent electrical characteristics of vertically aligned carbon nanofiber (CNF) arrays for on-chip interconnect applications. The study consists of three parts. First, the electron transport mechanisms in these structures are investigated using *I–V* measurements over a broad temperature range (∼4.4 K to 350 K). The measured resistivity in CNF arrays is modeled based on known graphite two-dimensional hopping electron conduction mechanism. The model is used because of the disordered graphite structure observed during high-resolution scanning transmission electron microscopy (STEM) of the CNF and CNF–metal interface. Second, electrical reliability measurements are performed at different temperatures to demonstrate the robust nature of CNFs for interconnect applications. Finally, some guidance in catalyst material selection is presented to improve the nanostructure of CNFs, making the morphology similar to multiwall nanotubes.**

***Index Terms*—Carbon nanofiber, interconnects, via.**

I. INTRODUCTION

CARBON-BASED nanostructures such as carbon nanofibers (CNFs) and carbon nanotubes (CNTs) have recently been investigated as candidate materials to replace key components in silicon-based devices. These components include transistors [1], [2], vias [3], [4], and other on-chip interconnects [3], [5]. In particular, for on-chip interconnect vias, state-of-the-art copper vias may suffer from increasing processing difficulties such as forming high-aspect-ratio trenches, achieving void-free copper filling, and depositing highly conformal barrier layers for the 32 nm node and beyond. Carbon nanostructures have been selected because of their robust electrical [4], [6], [7], thermal [8], and mechanical properties [9], [10]. Development of detailed simulation platforms to predict the benefit of using carbon nanostructures as on-chip interconnects (using Cu technology as a benchmark) has been demonstrated, but these studies have yet to come to a consensus as to whether the opportunity for implementation lies in local [11], intermediate, and/or global interconnect lines [12], [13]. In addition, the opportunity to integrate copper interconnects and CNT bundle vias is discussed as a method for increasing electromigration (EM) lifetime for interconnect structures as a result of the high thermal conductivity of CNTs. These simulations provide key metrics and considerations such as the effect of bundling, geometric factors, and contact resistance for future experimental work.

While contact resistance of CNF structures has been examined for via technology, the intrinsic properties of nanofibers for integrated circuit applications have yet to be fully explored [6], [14]. This work focuses on the study of fundamental electrical properties of CNF devices for use in on-chip interconnect and via applications. The two-dimensional (2-D) disordered morphology of graphitic layers defines the key difference between CNTs and CNFs. While defects in carbon nanotubes are characterized at an atomic level (dislocations and impurities in the hexagonal lattice), the unique structure of carbon nanofibers can be characterized macroscopically by investigating the thermal activation transport within the CNF. Fig. 1 shows the morphological differences between a carbon nanotube and carbon nanofiber. While the nanofiber exhibits a stacked cone morphology defined by a finite cone angle α, an ideal nanotube has a cone angle of zero degrees. Despite the defective morphology of nanofibers as compared to nanotubes, the plasma-enhanced chemical vapor deposited (PECVD) CNFs used in this work exhibit inherent fabrication advantages over multiwall CNTs because of the ability to grow at lower temperatures and superior vertical alignment. The structure investigated here presents a novel processing paradigm shift, using a bottom-up approach for interconnect via fabrication [5], and has the potential to become a viable alternative to the copper damascene process.

We aim to elucidate key electron conduction mechanisms in CNFs through low-temperature measurements. A recent study [15] predicted that given the conical nature of nanofibers, a graphitic plane charge transport model based on cone angle, or the angle that a graphite plane makes with respect to the direction of current flow, can be used to predict the resistivity of the material. Expanding on this model, including temperature dependence, we are able to predict conductance for a broad range of temperatures (∼4.4 K–350 K). We find that transport through the CNF can be described by an activated transport model, similar to the mechanism found in disordered systems [16]. We find that the cone angle at the base of the CNF generally defines its

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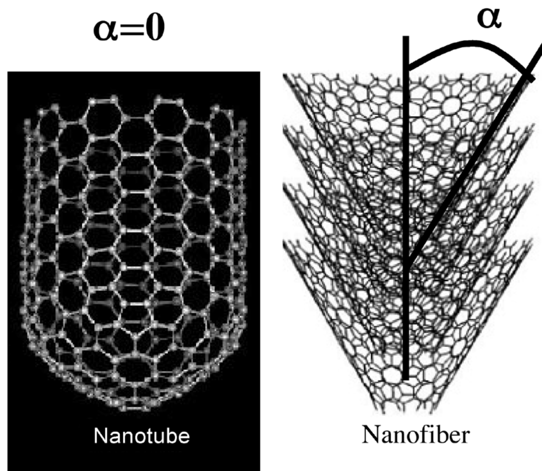

Fig. 1. Structural differences between carbon nanotube and carbon nanofiber produced by plasma enhanced chemical vapor deposition. In ideal carbon nanotubes, $\alpha = 0$.

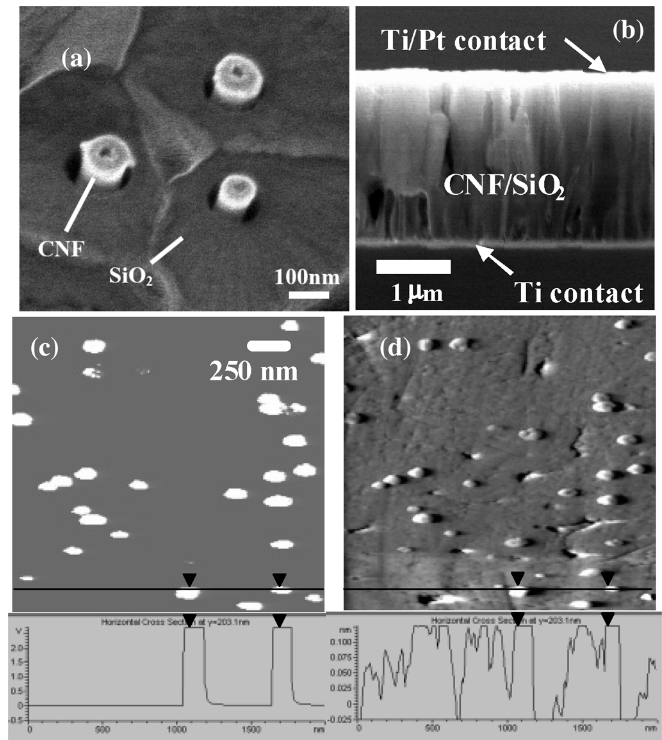

Fig. 2. (a) CNFs embedded in SiO_2 matrix. (b) Cross-sectional view of vertically aligned CNFs in SiO_2 matrix after contact deposition showing both contact electrodes. (c) Current sensing and (d) deflection AFM images of vertically aligned CNFs; the black arrows indicate the traces corresponding to the presence of protruding nanofibers.

transport. With $\alpha = 90°$ at the base, we expect hopping transport to dominate the temperature-dependent conductance [17], [18]. CNF growth and test structure fabrication are summarized in Section II. The model and measurement of CNF arrays at low temperature is presented in Section III. Reliability measurements were performed at an elevated temperature (90 °C) to demonstrate the robust nature of the CNFs under high-current stress conditions. Since electromigration (EM) has become a concern related to copper reliability, it is prudent to investigate these characteristics for next-generation materials. The results of room and elevated-temperature measurements are presented in Section IV. In Section V, Pd is explored as a catalyst material that improves contact morphology, ultimately improving resistance in the CNF structure. Initial transmission electron microscopy (TEM) characterization of Pd-catalyzed nanofibers also shows a vertically aligned array similar to the Ni-catalyzed case [19]. Electrical measurements and high-resolution scanning transmission electron microscopy (STEM) have recently shown the merits of using Pd as both a contact [20] and catalyst material [18].

II. Materials Preparation

Vertically aligned, freestanding CNF arrays were prepared for these measurements based on the conditions as presented in [21]. PECVD nanofibers were grown from a 35 nm thin film of Ni on a 30 nm Ti electrode deposited on silicon. For Pd-catalyzed nanofibers, a 20 nm thin film is used on a 30 nm Ti electrode deposited on silicon. Thus far, the alignment of the array has not been linked with growth temperature; however, alignment can be improved with the increase of plasma power during growth [22]. While temperature was not measured directly during the plasma growth process for Ni or Pd, anecdotal evidence concludes that a lower density plasma is sufficient for Pd-catalyzed growth of CNFs as compared with Ni [19]. Lower plasma power density leads to a reduction in ion bombardment of the sample/substrate [21], resulting in a lower growth temperature.

The CNF array was then encapsulated in SiO_2 using a low-pressure CVD process with tetraethylorthosilicate (TEOS) as an oxide precursor and subsequently polished, exposing approximately 30–50 nm of the CNFs [5]. The oxide encapsulation process ensures electrical isolation between CNFs and structural robustness of the array during mechanical polishing. The polishing process ensures removal of the catalyst particle at the CNF tip and a smooth oxide surface on which to deposit the contact electrode and to inspect the structure using current sensing atomic force microscopy (CSAFM). The resulting structure is shown in Fig. 2(a). By exposing a small portion of the CNFs at the tip, better contact can be made with the Ti/Pt contact pad deposited on top of the structure. Fig. 2(b) shows the final structure for both low-temperature and reliability measurements. Inspection of the sample surface by CSAFM is shown in Fig. 2(c) and (d). Fig. 2 demonstrates the conformal and uniform gap fill accomplished using the TEOS CVD process [5].

III. Temperature Dependent Electrical Characteristic of CNF Arrays

Multiwall CNT (MWNT) structures have been investigated for interconnect via applications [4], [23]. However, they have been shown to produce spaghetti-like structures not suitable for making reliable contact to the top electrode of the structure. The nanofiber array structures presented in this work have advantages over thermal CVD multiwall nanotubes because of the inherent vertical alignment of the array due to an applied electric field during growth, and lower growth temperature. The vertical alignment and freestanding nature of the nanofibers are demonstrated by SEM and CSAFM (Fig. 2). No physical interaction between neighboring CNFs has been observed before or after oxide encapsulation. This is an especially important fact when

TABLE I
COMPARISON OF RECENT REPORTED DC MEASUREMENTS OF CNT AND CNF VIAS

Reference (year)	[4] (2006)	[25] (2006)	[23] (2004)	[6] (2006)
Material	MWNT Bundle	MWNT Bundle	Single MWNT	Single CNF
Via Diameter [nm]	2000	700	20	50
Via Height [nm]	350	1000	150	4000
Resistance [Ω/via]	0.59	1.2 k	7.8 k	9 k (Pd), 13 k (Ni)
Resistivity [Ω-cm]	---	---	1.4 x 10^{-3}	4.4 x 10^{-4}, 6.3 x 10^{-4}
J_{MAX} [A/cm^2]	2.0 x 10^6	Not reported	5 x 10^8	>1 x 10^7

measuring single nanofiber electrical properties. The CNF array structures measured in this work are 50–100 nm in diameter and 3–4 μm in length, as shown in Fig. 2. The exposed tips are metallized with a contact pad (20 nm Ti/40 nm Pt) formed using ion-beam sputtering at 8 kV accelerating voltage and 4 μA beam current. Our aim is to use this structure to investigate the intrinsic conductivity limit of nanofibers through the use of modeling and measurement of low-temperature characteristics.

Our previous room-temperature measurements of 50 nm diameter vias reveal resistance values of 13.3 ± 3.0 kΩ for Ni-catalyzed CNF vias and 9.0 ± 1.6 kΩ for Pd-catalyzed CNF vias [18]. Further analysis of the resistance data using a Student's T distribution (number of samples: $N = 25$ for Ni and $N = 18$ for Pd) shows that the Ni and Pd-catalyzed resistance distributions will not overlap up to a 99% confidence level. In comparison to other work by Sato *et al.* [24], Choi *et al.* [25], and Kreupl *et al.* [3], the resistance measured at room temperature is higher in our material. Caution needs to be taken, however, when comparing resistance values, as they can only be directly compared when the geometries are identical. Comparing resistivity allows us to normalize the resistance values with respect to the geometry of the via.

Table I shows a summary of recent carbon nanostructure devices investigated as on-chip interconnect vias. A trend that can be seen from Table I is that most carbon nanostructure vias are capable of carrying well beyond the amount of current density that is necessary for next-generation interconnects. It should be noted that in the MWNT bundle cases [24], [25], no estimate for contact area is made (i.e., contact being made to nanotubes), so resistivity values cannot be calculated. One possible factor that affects resistivity of carbon nanofibers is the nanostructure of graphitic sheets at the CNF–metal interface. Fig. 3(a) shows the base of a 20 nm diameter CNF exhibiting graphitic sheets that are almost perpendicular to the axis of the nanofiber. Electrons would likely have to hop between graphite planes, which are not equally spaced because of the disorder, to conduct along the axis for this CNF–metal arrangement. Since the walls are not parallel to the axis, electron conduction cannot take place purely within the basal planes of graphite, as one would expect from a pure multiwall CNT. Further up the nanofiber, the alignment of graphite planes tends to form a cup-shaped morphology [18]. For each CNF, using high-resolution STEM, we can visually estimate the cone angle of the nanofiber from base to tip. The cone angle variation for a typical CNF can be seen in Fig. 4, where α rapidly approaches 90° at the base. The structure analyzed in Fig. 4 has been removed from the substrate, while previous studies have shown that when the nanofiber remains on the substrate, the cone angle is essentially 90° at the CNF–metal interface [17], [18]. With this structural characteristic in mind, we will present the low-temperature data, and revisit the interface properties as a basis for the accompanying model.

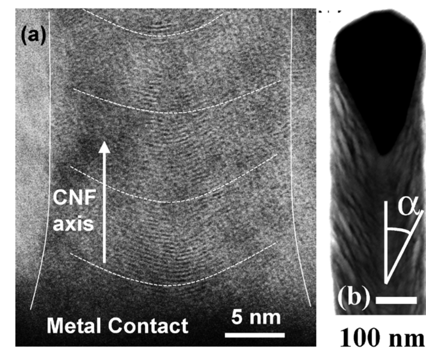

Fig. 3. (a) Nickel-catalyzed CNF showing graphite sheets with large α near the CNF–metal interface. (b) Cup-shaped morphology at the tip of a CNF.

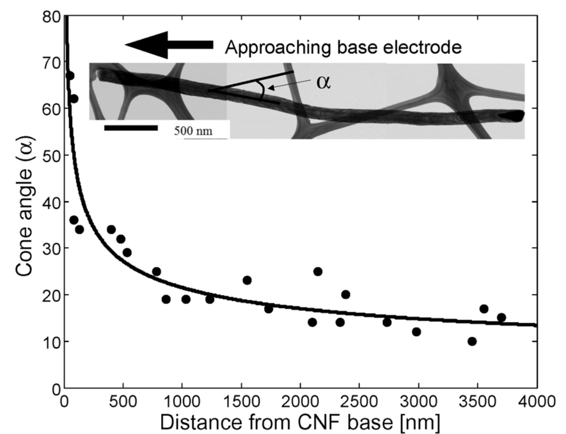

Fig. 4. Cone angle variation along the length of a typical CNF. The solid line is a best-fit line through the data (power law dependence $n = -0.34$). The cone angle reduces to between 10° and 20° approaching the CNF tip. Inset: SEM image of a 4 μm long nanofiber.

Low-temperature DC characteristics were measured using a wafer probe station with a two-terminal configuration. The

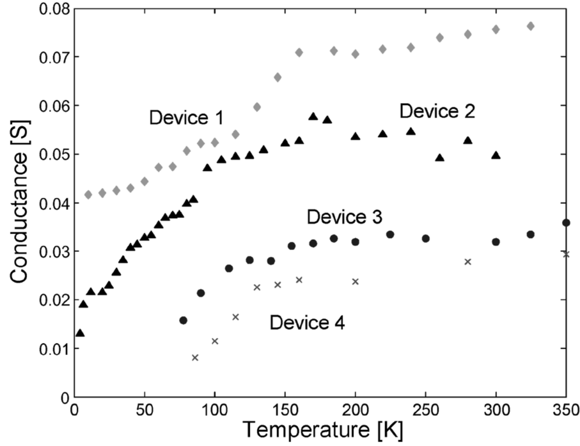

Fig. 5. Measured temperature-dependent conductance for a CNF via embedded in SiO_2 [structure shown in Fig. 2(b)].

chamber was evacuated and cooled to ~4.4 K (using liquid He) or 78 K (using liquid N_2), and a stage heater was used to slowly bring the sample temperature beyond 300 K. At intermediate temperatures, *I–V* characteristics were measured to obtain the via resistance. Fig. 5 shows the temperature-dependent conductance of four separate CNF array vias. For all devices, there are two common characteristics: 1) a monotonically increasing conductance at low temperature and 2) saturation of conductance above approximately $T = 150$ K. This saturated behavior holds up to at least $T = 500$ K (data not shown). This is relevant since moderate to high temperature is the expected operating range of the device, where metallic behavior is expected for interconnect applications.

In modeling the temperature-dependent behavior of each device, two main conductance values were taken into account, intrinsic CNF conductance, G_{CNF}, and contact conductance, G_i (or contact resistance, R_i). G_{CNF} represents the electron transport within a CNF via and we believe that our fabricated vias have some common physical transport mechanisms from sample to sample, since all are fabricated using the same process conditions. Thus, the intrinsic CNF wire conductance is assumed to be ohmic, i.e., $G_{\mathrm{CNF}} = \sigma_{\mathrm{CNF}} S_{\mathrm{CNF}}/L_{\mathrm{CNF}}$, where σ_{CNF} is a sample-dependent material property and S_{CNF} and L_{CNF} are the effective CNF wire cross-sectional area and length, respectively. R_i is inversely proportional to the contact area S_i, and depends on how the CNF is contacted to the electrode, which is sample specific, i.e., there would be a sample-dependent atomic-scale gap (or electron potential barrier width) of a few Angstroms between the CNF and electrode [26], in addition to various surface chemical residues affecting the electrostatics at the interface. Taking these points into account, we obtain

$$G_{\mathrm{TOT}}(T) = \frac{1}{G_{\mathrm{CNF}}^{-1} + R_i} = \frac{1}{\left(\frac{\sigma_{\mathrm{CNF}} S_{\mathrm{CNF}}}{L_{\mathrm{CNF}}}\right)^{-1} + R_i} \quad (1)$$

It is emphasized that G_{CNF} is given by Ohm's law while R_i varies from sample to sample. At this time, even though there is evidence that the tip and base contact morphologies are quite different, making it likely that the two contact resistances are not equal, we do not attempt to differentiate between the two contact resistances in this study, and use a single variable, R_i.

Our STEM data at the CNF–metal base contact indicates that the cone angle approaches 90° [27], thus we postulate that the conduction in the system is dominated by this interface, and therefore is subject to disorder. We can now assume that the CNF via will have a thermal activation transport channel where conductance increases monotonically with temperature T. Because the measured conductance is not zero but stays finite at around 4 K, we assume that there is another conducting channel where conductance is a slow-varying function of T in our temperature range (~4.4 to 350 K) [28]. The former would correspond to hopping transport in a disordered media, while the latter corresponds to the nonactivation type transport in an ordered media limited by phonon scattering. This additional nonactivation type conduction channel is modeled in (2) as σ_0 (constant with respect to T for simplicity). In fact we have shown that there exists a finite conductance approaching the low temperature limit at about $T = 4.4$ K (Fig. 5). Thus, we propose

$$\sigma_{\mathrm{CNF}} = \sigma_0 + \sigma_{\min} \exp\left[\frac{-E}{kT}\right] \quad (2)$$

where E is an activation energy, k is the Boltzmann constant, and σ_0 and $\sigma_{\min}$ are sample-dependent constants with units of conductivity [S/m]. The sample-independent E and sample-dependent $\sigma_{\min}$ are critical in analyzing our data and in deducing possible transport mechanisms.

We assume that the temperature-dependent transport represented by $\sigma_{\min}\exp(-E/kT)$ is limited by trapped charge centers. Electrons flowing in the CNF are sometimes trapped by these centers. Once trapped, electrons must have certain activation energy to escape from them. We further assume that each trap center will have the same physical properties with the same activation energy, and only its density varies from sample to sample. Thus, E is sample independent, but $\sigma_{\min}$ is sample-specific. The activation energy, E is a fitting parameter chosen to best fit each of the four devices. Consistent with our assumption of a sample-independent E, the value chosen, $E = 26$ meV, accurately describes all of the measured devices. Fig. 6(a) shows a typical transmission image of a section of CNF. Given this data and our previously published microscopy studies [18], [27], it is possible that physical abnormalities that could serve as trap centers existing in the CNF and their number varies widely from sample to sample. Fig. 6(b) and (c) show a schematic view of the low $\sigma_{\min}$ case with a high trap center density and the high $\sigma_{\min}$ case with a low trap center density, respectively. These trap centers could be related to lattice defects, impurities (contaminations), local charge sites, or a combination thereof. At this point, however, it is unclear what physical attributes cause the formation of energy-activated trap centers.

For in-plane conductance G_{inv} through the disordered inversion channel of metal–oxide–semiconductor field-effect transistors (MOSFETs), we often use an activation-type formula such that $G_{\mathrm{inv}} = G_{\min}\exp(-E/kT)$. $G_{\min}$ [S] generally takes a value of ~10% of the quantum conductance (i.e., 0.1 e^2/h), or 2.4×10^{-5} S for 2-D MOSFET inversion systems [29], but since transport is not in-plane but across the planes in CNFs, we treat $\sigma_{\min}$ [S/m] as a fitting parameter.

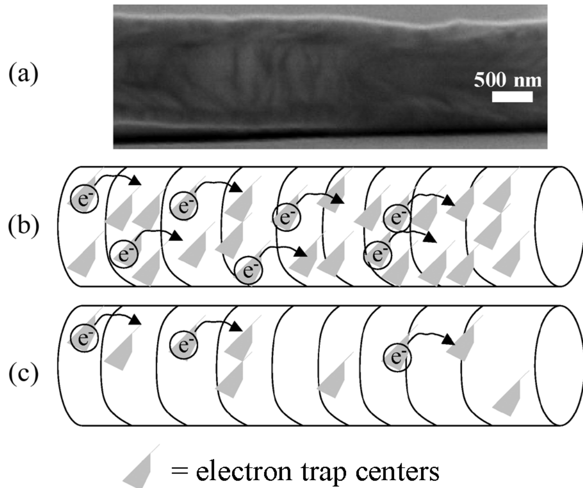

Fig. 6. (a) Transmission image of a section of CNF showing nonhomogeneous morphology along the CNF length. Schematic of sample exhibiting (b) high and (c) low electron trap center density due to physical anomalies, resulting in sample-dependent values of $\sigma_{\min}$ (2).

TABLE II
DEVICE FITTING PARAMETERS FOR EQUATION (1) TO FIT ALL FOUR TEMPERATURE-DEPENDENT MEASUREMENTS WITH A SAMPLE-INDEPENDENT ACTIVATION ENERGY $E = 26$ meV

	σ_0 [S/m]	σ_{min} [S/m]	R_i [Ω]
Device 1	8.29 x 10^{-2}	1.19	11.26
Device 2	4.16 x 10^{-2}	6.87	18.31
Device 3	1.39 x 10^{-4}	1.38	27.71
Device 4	9.59 x 10^{-5}	0.45	28.76

A summary of the device fitting parameters is shown in Table II. The fitted values are reasonably consistent among the four samples. $G_{\rm TOT}$ for each sample is accurately described using (1) with a sample-independent activation energy E, and sample-specific R_i. The fitting of the four devices with experimental data is shown in Fig. 7, demonstrating good agreement with (1). $\sigma_{\min}$, however, is orders of magnitude higher compared to the 2-D inversion value in MOSFETs [29] after appropriate scaling with $S_{\rm CNF}/L_{\rm CNF}$. This is not surprising considering the difference between the in-plane transport (MOSFET inversion) and transport across the planes (CNF). We note that $\sigma_{\min}$ is consistent with the Anderson localization model value [16], where an electron standing wave is formed because of quantum interference for an orbit connecting the relevant disorder sites at extremely low temperature. Our measurement temperature range is somewhat higher than where the Anderson model usually applies and at this stage, we do not understand whether this consistency is simply coincidental or has some physical meaning.

We can visualize (1) as the combination of the intrinsic CNF conductance and the contact resistance (conductance). For a typical device (Device 1), we can clearly see the two components' contributions to the overall conductance (Fig. 8). At high temperatures, the contact resistance is dominant as one would expect for nanotubes or nanofibers. This trend is quite consistent across all four samples.

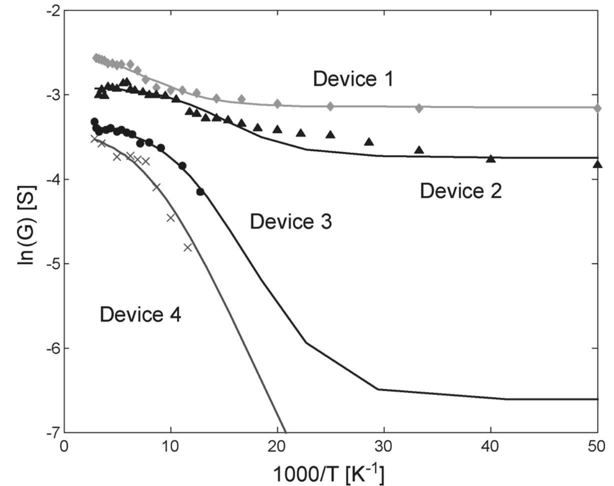

Fig. 7. Conductance fitting using equations (1) and (2) (solid lines) and measured data (symbols). Good agreement (maximum deviation is 20%) is obtained between model and measurement over the entire temperature range for all devices.

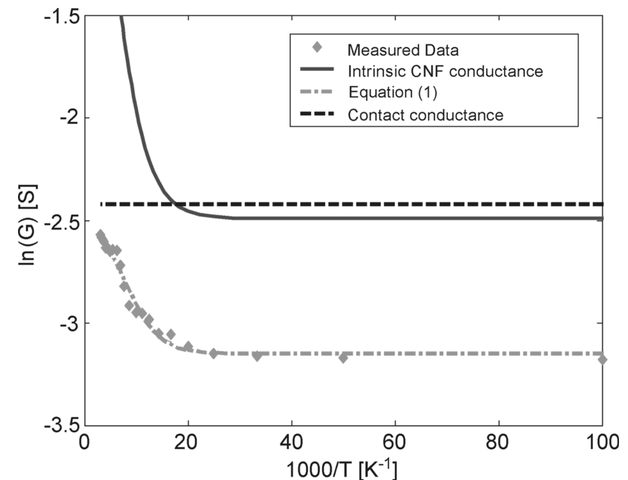

Fig. 8. Intrinsic and contact conductance components of total conductance for Device 1. Note that contact conductance dominates at high temperature.

IV. CNF ARRAY RELIABILITY

Next-generation copper via technology is expected to be severely limited by the amount of current that can be carried through the material to avoid failure due to EM. Nanoscale carbon structures are an attractive option to circumvent these difficulties as demonstrated in a previous study [7]. For the reliability measurement on CNF arrays in this work, the structure pictured in Fig. 2(b) is used. All electrical measurements are performed under high-vacuum conditions (1×10^{-6} torr). By passing high-current density through the CNF array structure using a constant voltage (1.5 V), electrical stress is applied to the system for over 160 h. The constant applied voltage in this experiment results in average current densities greater than 7×10^6 A/cm^2, above the required value for the 32 nm node ($> 4.3 \times 10^6$ A/cm^2) [30]. It should be noted that the contact area is calculated based on estimating the number of CNFs per unit area, and the CNF area from the diameter of each nanofiber (approximately 50–100 nm).

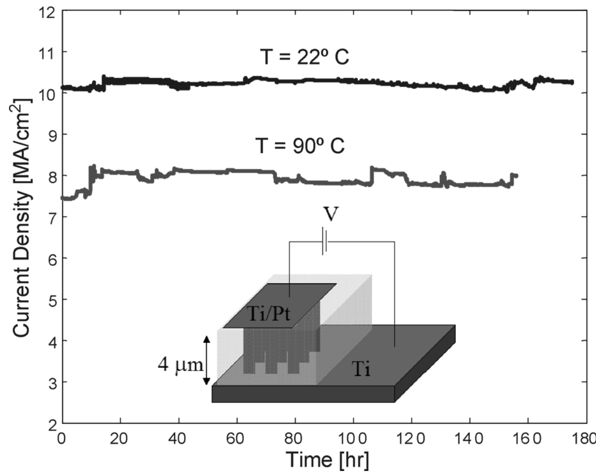

Fig. 9. High-current density stress results [6]. No degradation is observed over 160 h of constant-voltage (1.5 V) stress. Note that the contact area of the $T = 22^\circ$ sample is smaller than that of the $T = 90^\circ$ sample. Inset: Measurement configuration of high-current stress test.

The procedure for estimating the approximate number of nanofibers contacted using current sensing atomic force microscopy (CSAFM) is discussed in [5]. The results of the reliability tests are shown in Fig. 9 [6]. One sample is measured at room temperature (22 °C), while the other is measured at 90 °C with a larger contact area. From the results, no appreciable change over time is observed in the electrical characteristics of either sample other than some measurement noise caused by instrumentation, such as mechanical vibration and electrical noise, resulting in less than 8% fluctuation. *I–V* characteristics measured before and after the stress test show that there is no change in the ohmic behavior of the structure, indicating that there are no physical changes occurring in either the nanofibers or the CNF–metal contacts. Because these structures were not stressed to failure (due to instrumental limitations), we expect a higher maximum current density to be achieved. Based on these encouraging CNF reliability studies, we are currently conducting high-temperature (up to 200 °C) EM stress tests and fabricating via chains for more extensive systematic studies. In addition, these measurements will be performed in air to detect possible enhancement of CNF degradation. We expect similar results in air because of the protective conformal SiO_2 deposited around the nanofibers.

V. Catalyst Material Selection to Lower Resistance

The measurements presented in Sections III and IV were performed on CNF arrays grown using Ni catalyst for the PECVD process. The types of fibers produced have a contact morphology as seen in Fig. 3, which does not facilitate optimal conduction because of electron hopping between graphitic planes. Ideally, one would like to create a structure that resembles a MWNT, particularly in the base region, where the graphitic planes in the Ni-catalyzed structures exhibit the largest cone angles. One viable solution that has been proposed is the use of Pd as a catalyst material to improve CNF-contact morphology [18], therefore improving resistance. A typical Pd-catalyzed structure is shown in Fig. 10, where graphitic planes are almost perpendicular to the underlying Ti layer. This

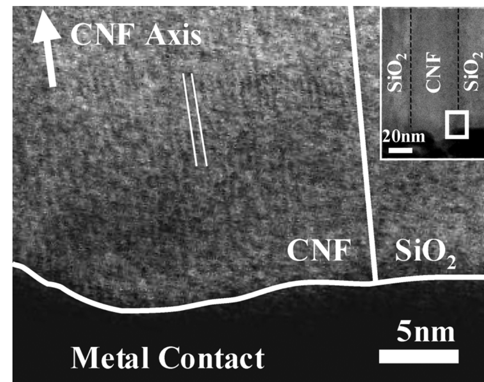

Fig. 10. High-resolution STEM of palladium-catalyzed CNF showing graphite sheets parallel to CNF axis characterized by high-resolution STEM. Inset: STEM image of Pd-catalyzed CNF embedded in an SiO_2 matrix. The white box indicates the area of high-resolution STEM analysis.

TABLE III
Resistance of 50 nm Diameter Ni- and Pd-Catalyzed CNFs

Type of CNF	Average Resistance (kΩ)	Average Resistivity (μΩ-cm)	Minimum Resistance (kΩ)	Minimum Resistivity (μΩ-cm)
Ni-catalyzed	13.0 ± 3.0	630 ± 150	8.6	422*
Pd-catalyzed	9.0 ± 1.6	440 ± 79	5.8	50**

* 50 nm diameter via	** 21 nm diameter via

morphology is favorable for electronic conduction because of the alignment of graphitic planes parallel to the overall direction of current flow. While the nanostructural morphology of Pd-catalyzed CNFs is vastly different from their Ni-catalyzed counterparts, the growth conditions, macroscopic morphology, and vertical alignment are all similar using these two catalyst materials. It is shown using CSAFM (to probe individual nanofibers) that Pd-catalyzed CNFs provide a lower resistance than similar Ni-catalyzed structures. Table III shows the resistance comparison between Ni and Pd-catalyzed structures. Both the average and lowest resistance values measured are listed, demonstrating the advantage of using Pd as a catalyst for CNF growth. The lowest resistance value (5.8 kΩ) measured in the Pd-catalyzed case corresponds to a resistivity of 50 $\mu\Omega - \mathrm{cm}$ for a 21 nm diameter, 4 μm long CNF. This result is roughly equivalent to the resistivity measured for a axis graphite, which ranges from 40 to 80 $\mu\Omega - \mathrm{cm}$ [31]. Comparing this resistance value (5.8 kΩ) to a model [32] for copper interconnect technology scaled down for a 21 nm diameter, 4 μm tall copper via, the CNF array via will not achieve the predicted 312 Ω. This prediction, however, assumes that the copper material will not undergo any catastrophic changes, such as those brought about by EM. In addition, grain boundary scattering and sidewall roughness scattering are not accounted for in the model [32] and will most certainly affect the resistance in this size scale. Nevertheless, improvements for CNFs are certainly necessary and possible in growth processes, catalyst optimization, contact interface engineering, and the development of novel processing schemes.

VI. CONCLUSION

In this work, we have investigated temperature-dependent characteristics of CNF arrays for on-chip interconnect applications. A model based on fundamental properties of disordered media is presented for the low-temperature behavior of CNF array vias to better understand electron conduction mechanisms in carbon nanofibers. Reliability results at room temperature and 90 °C are also presented, demonstrating the robust nature of the CNF array for interconnect via applications. Finally, Pd is demonstrated as a catalyst material that improves CNF-contact morphology and lowers overall resistance.

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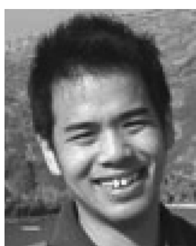

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