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Effect of improved contact on reliability of sub-60 nm carbon nanotube vias

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Abstract
Advances in semiconductor technology due to the aggressive downward scaling of on-chip feature sizes have led to rapid rises in the resistivity and current density of interconnect conductors. As a result, current interconnect materials, Cu and W, are subject to performance and reliability constraints approaching or exceeding their physical limits. Therefore, alternative materials are being actively considered as potential replacements to meet such constraints. The carbon nanotube (CNT) is among the leading replacement candidates for on-chip interconnect vias due to its high aspect-ratio nanostructure and superior current-carrying capacity to Cu and W, as well as other potential candidates. Based on the results for 40 nm and 60 nm top-contact metallized CNT vias, we demonstrate that not only are their current-carrying capacities two orders of magnitude higher than their Cu and W counterparts, they are enhanced by reduced via resistance due to contact engineering facilitated by the first reported contact resistance extraction scheme for a 40 nm linewidth.

Keywords: carbon nanotubes, contact resistance, metallization, interconnects, current-carrying capacity

(Some figures may appear in colour only in the online journal)

1. Introduction

For the past two decades, there have been unprecedented advances in semiconductor technology, guided by Moore's law and engineered by lithography-based scaling [1]. This has resulted in the aggressive downsizing of on-chip components such as transistors (active devices or front-end-of-line) and interconnects (passive devices or middle-of-line and back-end-of-line) [2]. Scaling transistor dimensions result in a reduction of the areas of gate capacitors and other parasitic capacitors. This enables transistors to operate with smaller voltage swings and faster charge/discharge or switching cycles. Therefore, scaling transistors improve their performance and reduce their power consumption as downward scaling continues [3]. On the other hand, scaling interconnects result in the shrinking of their cross-sectional areas, leading to a surge in resistivity as the electrons moving through the interconnect conductor experience increased scattering at the grain boundaries and surfaces of the conductor in the interconnect structure [4–8]. Also, reducing the interconnect dimensions results in an increase in the contact resistance as the electrons encounter smaller bottlenecks at the contacts. Therefore, the combined effect of increases in resistivity and contact resistance in the interconnects leads to higher resistance with downward scaling.

The performance metric of the interconnect is denoted by the delay time τ experienced by an electrical signal traveling through it, which is expressed as $\tau = RC$, where R = total equivalent resistance of interconnect lines, and C = total equivalent capacitance resulting from the interconnect lines and surrounding interlayer dielectrics (ILD) [9, 10]. A manufacturable W interconnect structure requires a TiN adhesion layer for the W deposit and for the structure to remain intact through the chemical mechanical polishing (CMP) step, as well as a W nucleation layer to facilitate low-resistivity bulk W growth and to prevent TiN etching by F^- radicals from the

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WF_6 precursor [11–14]. On the other hand, a manufacturable Cu interconnect structure comprises of a TaN/Ta barrier layer to prevent Cu diffusion in the ILD [15–17], and a seed layer of physical-vapor-deposited (PVD) Cu to provide nucleation for the subsequent electro-deposition to fill the Cu in the interconnect structure [18, 19]. The addition of these relatively high resistivity liners in either case results in a reduction of the total available volume for the conductor to fill the interconnect structure and hence increases the total resistance and τ. To offset this increase, the ILD with a lower dielectric constant k is employed in the interconnect structure to reduce the total capacitance. Even with such dielectric engineering, for a 90 nm node the transistor gate delay is 2.5 ps, while a Cu/low-k interconnect delay is 10 ps [3]. Therefore, the circuit performance is limited by that of the interconnects and not by the transistors [3]. As the current technology is well beyond the 90 nm node and approaching the sub-10 nm regime, the increase in Cu resistance continues to degrade the overall circuit performance.

With the continued downward scaling of interconnect dimensions, the conductor cross-sectional area is reduced, resulting in an increase in current density. Thus, the reliability of interconnects and their ability to withstand operating current densities for a particular node size is diminished [2]. Once the current density in an interconnect line exceeds the maximum current-carrying capacity J_{max} of the conductor, the material fails due to the displacement of atoms along the path of electrons, resulting in voids, and such a mechanism is known as electromigration. The J_{max} of Cu is 2.5 MA cm^{-2} [20] and 1 MA cm^{-2} for W [21, 22]. In order to extend the J_{max} for Cu and W, material engineering approaches such as stress engineering and capping are employed [2]. To implement such approaches, the Blech length [23–25], or the maximum length of the interconnect line at which the internal stress in the conductor can offset electromigration, is experimentally determined. Interconnect lines are then designed for lengths shorter than the Blech length [24, 26, 27] to prevent electromigration. In addition, capping layers are employed to cover the interconnect lines so that the conformal coating of such layers can provide an adhesive force for the conductor to counter electromigration. Combining these two approaches, the J_{max} of Cu can be extended to 3 MA cm^{-2} [2]; however, the current density for 10 nm nodes and beyond is expected to be well above this figure [2]. Therefore, it is critical to explore and evaluate alternative conductors to replace Cu and W for interconnects in order to meet both the performance and reliability requirements of advanced nodes.

In order to evaluate the candidates for replacing Cu and W in the interconnects of advanced nodes, materials with different electron mean free paths are considered, since Cu and W are susceptible to resistivity surges due to the increased electron scattering for nanoscale linewidths [28]. One approach is to identify conductors with an electron mean free path in the bulk that is much smaller than those of Cu and W. Such materials have higher bulk resistivities compared to Cu and W due to more electron–electron scattering. However, as these materials are scaled down to the nanoscale, surface scattering becomes the dominant contributor to resistivity [28]. Thus, they may exhibit resistivity comparable to Cu and W in the nanoscale regime. One example is NiSi, with an electron mean free path of ~5 nm [29, 30], compared to 40 nm for Cu [31]. NiSi was reported to have a resistivity of 19 $\mu\Omega$ cm for $<$30 nm linewidths—about four times that of Cu—and a significantly higher J_{max} of 10 MA cm^{-2} [30]. However, control of monosilicide phase formation throughout the conductor length is a major challenge in functionalizing NiSi interconnects.

Another approach is to identify materials with an electron mean free path that is much longer than those for Cu and W. For such materials, only interface scattering contributes to resistance because the electrons experience near-ballistic transport at sub-100 nm dimensions. An example is the multi-walled CNT (MWCNT) which can have an electron mean free path of up to 1 μm [32–34], as well as a J_{max} on the order of 100 MA cm^{-2} [35–39] due to its strong sp^2 C–C bonds. Because of its exceptionally high J_{max} and the potential of CNT-based nanostructures to achieve resistance comparable to or lower than their Cu and W counterparts, the CNT is the leading candidate to replace Cu and W in interconnect vias and contacts.

An MWCNT is made up of concentric cylinders, each one being a rolled-up sheet of graphene. Thus, its two ends exhibit unsaturated carbon bonds from each graphene sheet or shell suitable for making stable and low-resistance contacts. The two most common ways of growing CNTs in an interconnect via structure are by plasma-enhanced chemical vapor deposition (PECVD) and thermal CVD, both consisting of the catalytic decomposition of hydrocarbons on dewetted catalyst sites [40]. While PECVD utilizes plasma to maintain the vertical alignment of CNTs, for thermal CVD the alignment of the densely packed CNT is achieved with van der Waals forces among the neighboring CNTs [41]. Extensive experiments have conclusively demonstrated that growth temperatures in the 800 °C–1100 °C range lead to long-range order in CNTs and fewer defects [42], thus ensuring long electron mean free paths. In recent years, the CNT has been evaluated as a via material with various experimental foci, one being to integrate them into vias with a growth temperature of ~400 °C, compatible with a back-end-of-line thermal budget [43]. In particular, Katagiri [44–46] reported CNT vias 70 nm wide with an aspect ratio ~1, while Vollebregt [47] characterized CNT vias with a linewidth in the 1–4 μm range. However, further study is needed for sub-100 nm linewidths to ensure that the structures containing low-temperature CNTs meet the performance and reliability requirements. Chiodarelli [48] described a catalyst engineering scheme to reduce via resistance by increasing the CNT packing density inside vias, at a CNT growth temperature of 550 °C. However, the test device reported comprised of 300 nm vias without projections for smaller linewidths. On the other hand, Zhou [49] reported CNT via results for linewidths down to 60 nm and projected the resistance for a 30 nm via. Van der Veen [31] reported an electron mean free path for CNT approaching that of Cu in 150 nm vias. Graham [50] succeeded in fabricating a 30 nm CNT via with CNTs grown at 700 °C and further annealed to 850 °C during electrical measurement, but the reported via

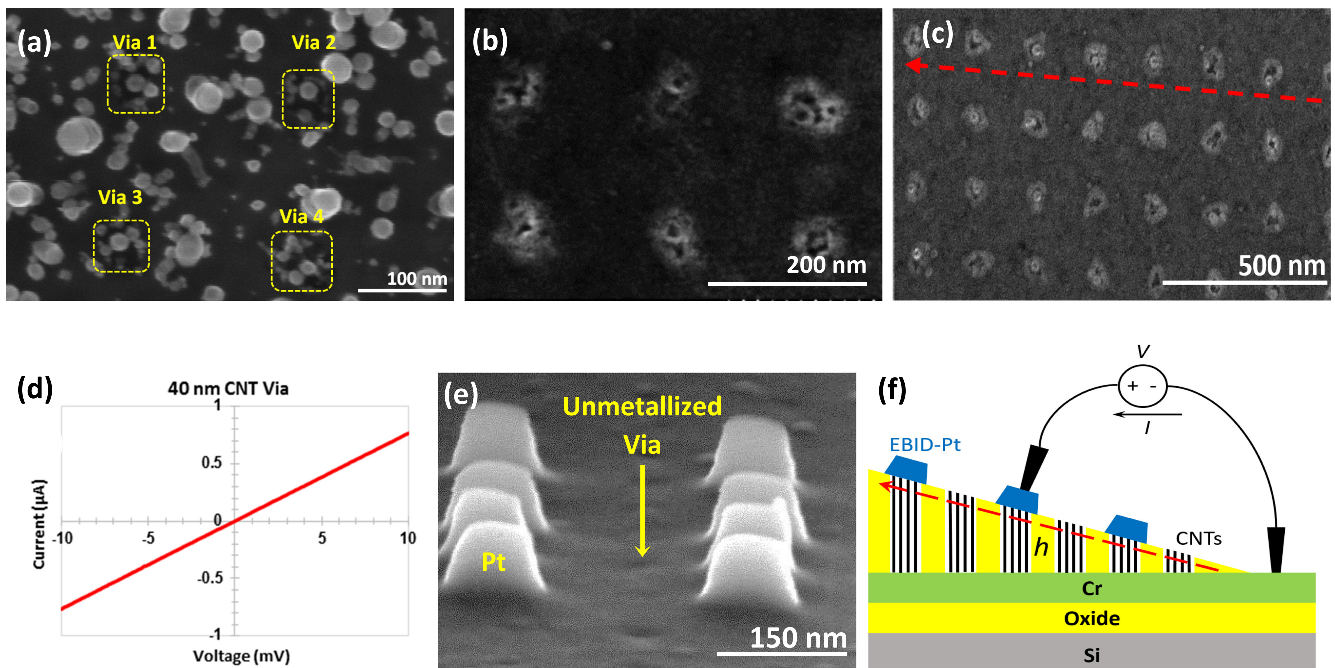

Figure 1. (a) Top-view SEM images of 40 nm vias after CNT growth. (b) CNT vias of 40 nm after Al_2O_3 filling and polishing. (c) Top-view of wedge formed after polishing and before EBID-Pt deposition. The arrow indicates the direction of the wedge from low to high. (d) Typical measured *I–V* behavior that yields via resistance R_{via} before EBID-Pt top-contact metallization. (e) Glancing view of CNT vias after EBID-Pt. Alternate vias are selectively metallized in order to avoid overlaps. (f) Cross-sectional schematic of wedge with nanoprobing setup showing varying via height h used for contact resistance extraction. The arrow indicates the direction of the wedge as in (c). (g) Cross-sectional TEM images of a row of 40 nm CNT vias with EBID-Pt top contacts, confirming that the lateral spread of the deposited Pt is limited to one via. The inset shows a stray a-C deposited on the field due to the organometallic precursor used in the EBID process. (h) High-resolution TEM image of a 40 nm via revealing a CNT with a diameter of ~5 nm.

resistance was two orders of magnitude higher than its Cu and W counterparts.

All of the above findings, while providing useful knowledge for further studies toward the realization of CNT vias, nevertheless share one common challenge: namely, controlling and minimizing the resistance between the CNT and the metal contacts to achieve an interconnect via resistance approaching that of Cu and W. Furthermore, the effect of via contact engineering on reliability as well as performance has not been addressed thus far. In this paper, we present a study to correlate CNT contact resistance with both the performance and reliability of 60 nm and 40 nm vias. We also examine the prospects of contact engineering in maintaining the CNT's superiority in reliability over all other materials, while continuing to improve its performance to approach that of Cu and W, in the quest to be the interconnect material for end-of-roadmap semiconductor technology nodes.

2. Device fabrication and characterization

Via structures with 60 nm × 60 nm and 40 nm × 40 nm cross-sections and 130 nm and 80 nm heights, respectively, are patterned using electron-beam (e-beam) lithography and reactive ion etching, as previously reported [49]. In order to enable the catalyst-assisted PECVD tip-growth of the CNTs inside the vias, a 3 nm Ni blanket deposition is carried out using e-beam evaporation [49]. Figure 1(a) shows the top-view SEM image of the 40 nm vias after CNT growth. As the Ni catalyst was deposited on the entire sample, this results in the growth of stray CNTs around the vias as well. To obtain the areal density, the number of CNTs in each via before dielectric filling and polishing is counted. This method takes into account all the CNT tips observed from the SEM images, some of which may not emerge from the dielectric filler upon polishing to be part of the via top-contact. Therefore, this method provides an upper limit for the CNT areal density. The as-grown CNT areal density obtained in a 40 nm × 40 nm via is $\sim 10^{12}$ cm^{-2}. To prepare vias for subsequent top-contact metallization, it is necessary to fill the interstices inside each via to avoid the shorting of the top and bottom contacts. To achieve this, a 6 nm conformal Al_2O_3 film using atomic layer deposition is used. The sample is then subjected to mechanical polishing using SiO_2 nanoparticle slurry to make contact with the sample at an angle in order to fashion a ~1° wedge on the surface. The top-view SEM images of a few vias after polishing, and of the resulting wedge are shown in figures 1(b) and (c), respectively. Such a wedge allows one to measure vias with different heights on the same sample and extract contact resistance, with all the devices grown under the same process conditions, thus minimizing process variations. An area of Cr underlayer is exposed near the wedge using a focused ion beam (FIB) that serves as the ground for the measurement. To ensure that the oxide coating on the CNTs is removed and the CNT shells are exposed after polishing, a preliminary test is performed on a few vias with a typical *I–V* behavior shown in figure 1(d),

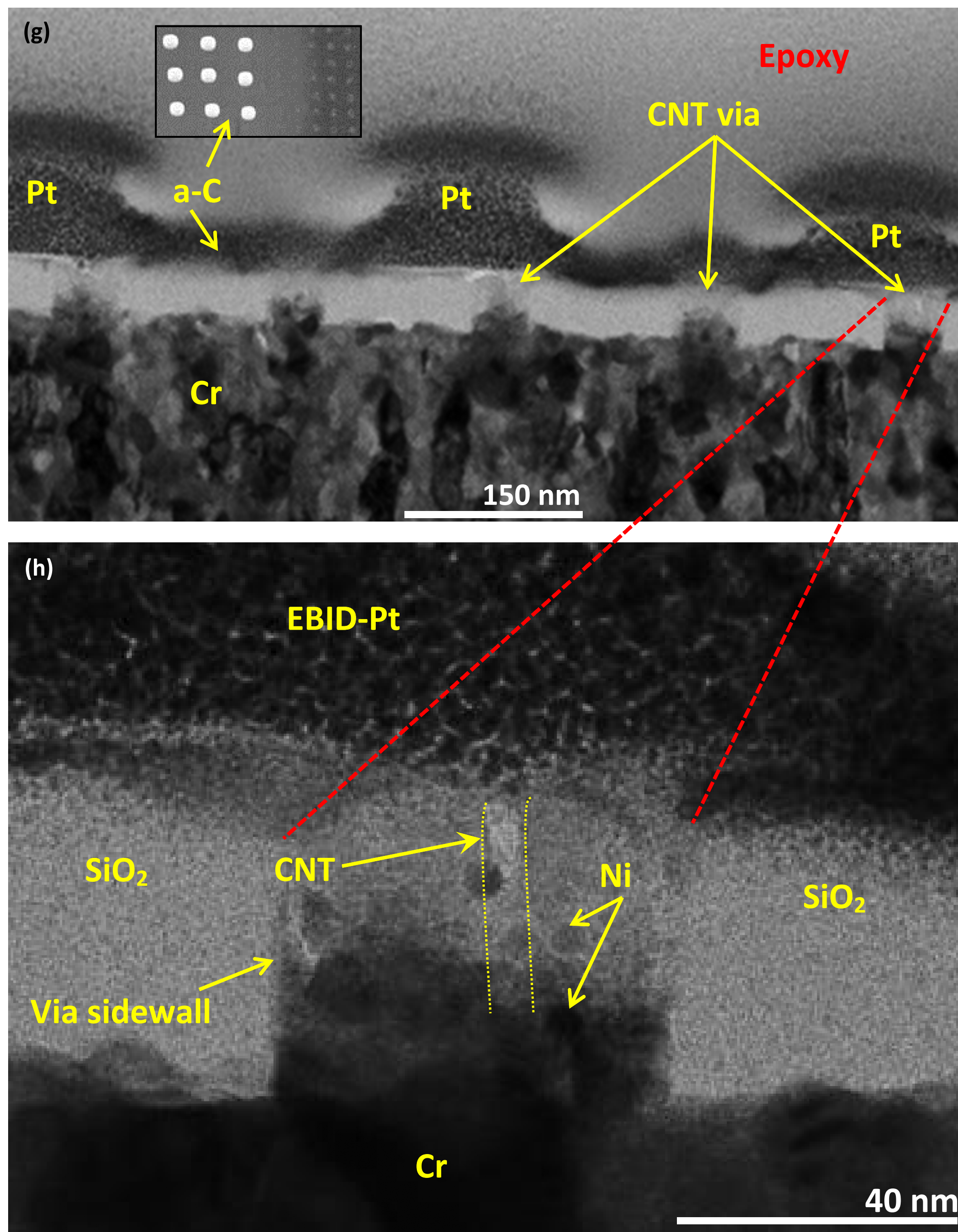

Figure 1. (Continued.)

confirming ohmic conduction. The corresponding resistance of 13 kΩ for this 40 nm via falls within the range projected from measurements on CNT vias with widths ranging from 150 nm to 60 nm that were fabricated using similar process conditions [49].

To reduce measurement variations among the vias and to improve the CNT-metal contact, the via top-contacts are metallized for each of the five different via heights using the electron-beam-induced deposition (EBID) of Pt in an SEM chamber. EBID enables us to selectively deposit Pt on top of the vias without any additional masking steps. Deposits with fine control can be made using EBID with no damage to the substrate, unlike using a focused ion beam (FIB), which generally creates defects and Ga contamination [51]. For EBID, a base pressure of 10^{-3} Pa is reached before the Pt precursor, trimethyl(methylcyclopentadienyl)platinum(IV), is introduced using a gas injection system (GIS). An advantage of using a non-halide precursor is that it does not lead to substrate damage from the dissociated halide radicals. Prior to Pt deposition, the sample is placed in the chamber for an hour to allow outgassing to occur. This step is critical in ensuring that oxide-free depositions are made on the vias. The chamber is then subjected to plasma cleaning to purge potential contaminants on the chamber walls, especially a-C, and to clean

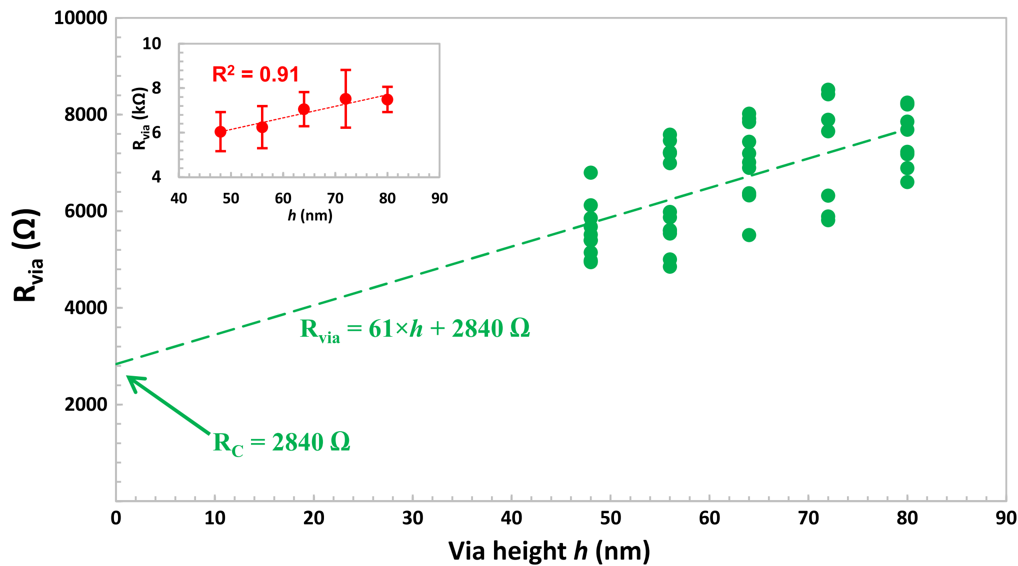

Figure 2. Measured via resistance versus via height for 40 nm CNT vias. Statistical linear fitting of the data yields the *average* contact resistance R_C from the R_{via} intercept. The inset shows the mean and standard deviation of measured resistances for each via height with $R^2 = 0.91$. The data further supports ohmic transport through the entire via structure.

the sample surface to further expose the CNT tips. The cleaning efficiency can be checked by using an irradiating e-beam on the sample for 5 min to ensure no a-C remains.

For EBID, the working distance is set at 10 mm and the accelerating voltage at 10 kV, with an emission current of 80 pA. The Pt precursor is delivered from the GIS through a needle outlet which is kept at 3 $\sim$ 4 mm from the sample surface. The e-beam dissociates the precursor molecules and yields Pt deposition on the impinged spot (via) on the sample surface. The lateral beam spread causes the deposit to be somewhat larger than the targeted spot. The beam raster time on each via is 1 s for a 90 nm $\times$ 90 nm spot to cover a 60 nm $\times$ 60 nm via. Depositions with a longer raster time result in significantly wider lateral spreads, which can lead to deposits on the adjacent vias and skewed *I–V* data. Alternate vias along the same row are metallized to ensure no overlaps of Pt deposits due to lateral beam spread. Multiple vias for each height are metallized to yield sufficient data for the subsequent statistical analysis. An SEM image of two rows of metallized vias sandwiching an unmetallized one is shown is figure 1(e). A schematic for the *I–V* measurement of vias with metallized top contacts on the fashioned wedge is illustrated in figure 1(f).

Figure 1(g) shows a TEM cross-section of several 40 nm CNT vias along a row of the wedge. It indicates that the alternate vias are metallized and confirms that the Pt deposits do not overlap. The presence of a-C from the organometallic Pt precursor is evident but is shown to be not sufficiently conductive to create a significant conducting path between the adjacent vias. Figure 1(h) is a high-resolution TEM image of a single CNT via. The vias are designed for a horizontal cross-section of 40 nm $\times$ 40 nm, while the vertical cross-section traversed by the transmitted electron beam producing the image can be as wide as $40\sqrt{2}$ or 57 nm. Furthermore, etching in the via patterning process can result in horizontal cross-sections that might not be perfect squares. The fact that only one CNT is clearly visible is a result of ion milling creating a sufficiently thin sample—usually less than 50 nm thick. Thus, it is not likely that most of the CNTs observed in the top-view SEM image in figure 1(b) are present in such cross-sectional views of the very thin slice. Nevertheless, the observed CNT in figure 1(h) reveals alignment with the via sidewalls and interfaces with both the underlayer Cr and Pt top-contact, similar to findings for a 60 nm via [49].

3. Contact resistance and current-carrying capacity measurements

The electrical characterization of CNT vias was carried out by nanoprobing vias with metallized top-contacts, as shown schematically in figure 1(f). One nanoprobe makes contact with the Pt cap while the other rests firmly on the area of exposed Cr serving as the ground. The Cr underlayer is 300 nm thick, which ensures minimal contribution to the total via resistance. In fact, the sheet resistance of the Cr layer measured before oxide deposition is 3.2 $\Omega/\Box$. After the initial *I–V* sweep to confirm conduction and ensure the firm mechanical contact of the nanoprobe with the Pt cap, the CNT via is subjected to current stressing starting at 1 μA in multiple cycles, until the resistance stabilizes. This simple contact engineering technique further improves the top-contact through joule heating, as no thermal treatment is performed after EBID deposition. Significant improvement in the CNT via resistance by thermal annealing has been reported [31, 50]. In particular, Graham [50] reported a resistance drop by over two orders of magnitude with annealing up to 850 °C. In our experiment, instead of thermally annealing the entire sample, current stressing of the individual CNT vias is performed, as in horizontal CNT interconnects [51]. The resistance is recorded after each stress

cycle, and the final value is obtained when no reduction in resistance occurs with further stressing. Multiple via resistances for each of the five different via heights using the technique illustrated in figure 1(f) are plotted in figure 2.

The range of via heights is selected such that the lowest height is at least half the maximum via height in order to avoid the accidental shorting of the top and bottom electrodes. Since the via height range is 48–80 nm, as shown in figure 2, the electron free path is at most 80 nm through the CNTs inside each via. Nevertheless, the transport through the entire via structure is assumed to be ohmic, which is the basis of the ensuing analysis. Each via resistance R_{via} can then be expressed as

$$R_{via} = R_m + R_C + \rho_{CNT} \times h/A_{CNT}. \quad (1)$$

R_m represents the total resistance contributions from the Cr underlayer, probes, and probe-Cr contacts, and its value is estimated by landing both the nanoprobes on the exposed Cr area. The typical value obtained is $\sim 10\,\Omega$, which is $<0.2\%$ of the lowest measured R_{via}. Hence, R_m can be neglected in the subsequent analysis. R_C is the total contact resistance of the via and varies among them according to the number and diameter of the CNTs inside each via. A_{CNT} is the total CNT cross-sectional area inside the via and also varies among them. Such variations are manifested in the data spread for each via height shown in figure 2. The via height h is fixed among vias of the same height using the wedge structure shown in figure 1(f). While the CNT resistivity ρ_{CNT} depends on the number of defects in the graphitic structure and number of walls, relative to the variations of A_{CNT} and R_C among the vias (to be addressed in the ensuing paragraph), and considering the small range of via heights used, the variation in ρ_{CNT} among them is expected to be small, and an average value for the sample is assumed in the analysis. Thus, in using equation (1) to extract the contact resistance from R_{via} versus the h data, the resistance intercept of the statistical linear fit amounts to an average R_C that takes into account all variations among the vias. The fitted line has a slope of $61\ \Omega\ \text{nm}^{-1}$ with $R^2 = 0.91$, supporting the assumption that conduction through the entire CNT via structure is indeed ohmic, with an average CNT linear resistivity $\rho_{CNT}/A_{CNT} = 61\ \Omega\ \text{nm}^{-1}$. The mean R_{via} and standard deviation for each h are given in the inset in figure 2. Therefore, despite significant variations among the vias, such statistical analysis can be employed to extract an average via contact resistance and an average CNT resistivity, with $R_C = 2.8\ \text{k}\Omega$ and $\rho_{CNT} = 1.8\ \text{m}\Omega\ \text{cm}$, where an average $A_{CNT} \sim 300\ \text{nm}^2$ is obtained by sampling a large number of 40 nm vias. This resistivity value is an order of magnitude lower than the ones obtained for the lower CNT growth temperature [47], but still more than two orders of magnitude higher than Cu and W with similar linewidths [11–13].

To examine the variations among vias further, a statistical analysis is performed on the variations in the diameter and number of CNTs inside each via, as well as the resulting variations in the extracted contact resistance. The diameters and number of CNTs making contacts with the top and bottom electrodes define the total conducting cross-sectional area in a via, and variations in that area among the vias manifest themselves in variations in the measured R_{via} and extracted R_C. For the set of vias used in this experiment, the mean (μ), standard deviation (σ), and coefficient of variation (CV) for each of these parameters are summarized in table 1.

Table 1. Statistics of 40 nm CNT via parameters which contribute to variations in the measured via resistance and extracted contact resistance. For the diameter and number of CNTs, the data is obtained from the SEM images of unfilled and unpolished vias, such as figure 1(a), whereas the total CNT area in the via is obtained from the SEM images of polished samples such as figure 1(b). For each parameter, the mean μ, standard deviation σ, and coefficient of the variation CV are obtained, showing similarities in the variations for A_{CNT} and R_C.

Parameter in a set of 40 nm CNT vias	μ	σ	CV(%)
CNT diameter across the entire set (nm)	9.03	3.62	40.1
Number of CNTs in via, N_{CNT}	16	2	12.5
Total area of CNTs in via, A_{CNT} (nm^2)	310	101	32.6
Extracted R_C (kΩ) from figure 2	2.84	0.8	28.6

For CNT vias exhibiting the ohmic conduction described by equation (1), both contact resistance and the total CNT resistance are inversely proportional to A_{CNT}. Thus, one would expect the extracted R_C to have variations similar to those in A_{CNT}, as shown in table 1. If we were to use the average CNT diameter and number given in table 1 to deduce the average A_{CNT}, it would be $\sim 1000\ \text{nm}^2$. This value is clearly an overestimation as both the SEM and TEM images of the unpolished vias in figure 1 reveal CNTs with lengths lower than the via heights, which do not contribute to conduction. On the other hand, the presence of the oxide surrounding the vias as well as the exposed dielectric filler material in the polished sample results in insufficient contrast for accurate individual CNT diameter and number determination, but adequate for the total area estimation. The resulting A_{CNT} statistics given in table 1 match well those for R_C, thus validating the analysis used to extract the latter.

We have recently demonstrated the advantage of integrating CNTs at temperatures higher than those considered to be acceptable for IC manufacturing, where the resulting high CNT quality leads to lower resistivity and higher current-carrying capacity [52, 53]. To obtain CNTs via current-carrying capacity J_{CNT}, two complementary methods are employed. For the first method, a constant current is applied to the via in incremental steps and the resistance is recorded after each stress cycle until device breakdown. This is similar to reports on studies for horizontal CNT interconnects [54, 55]. The resistance versus stress current behavior for 40 nm and 60 nm CNT vias with and without a Pt cap are shown in figures 3(a) and (b), respectively. It is observed that the via with the Pt top-contact can carry much higher current than the one without, with reduced via resistance. The Pt contact allows all the exposed CNT tips and the graphene shells inside each CNT to interface with the deposited metal, whereas for vias without the metallized top-contact, via resistance is very sensitive to variations in probe-via contact, which generally does not cover all the CNTs inside the via,

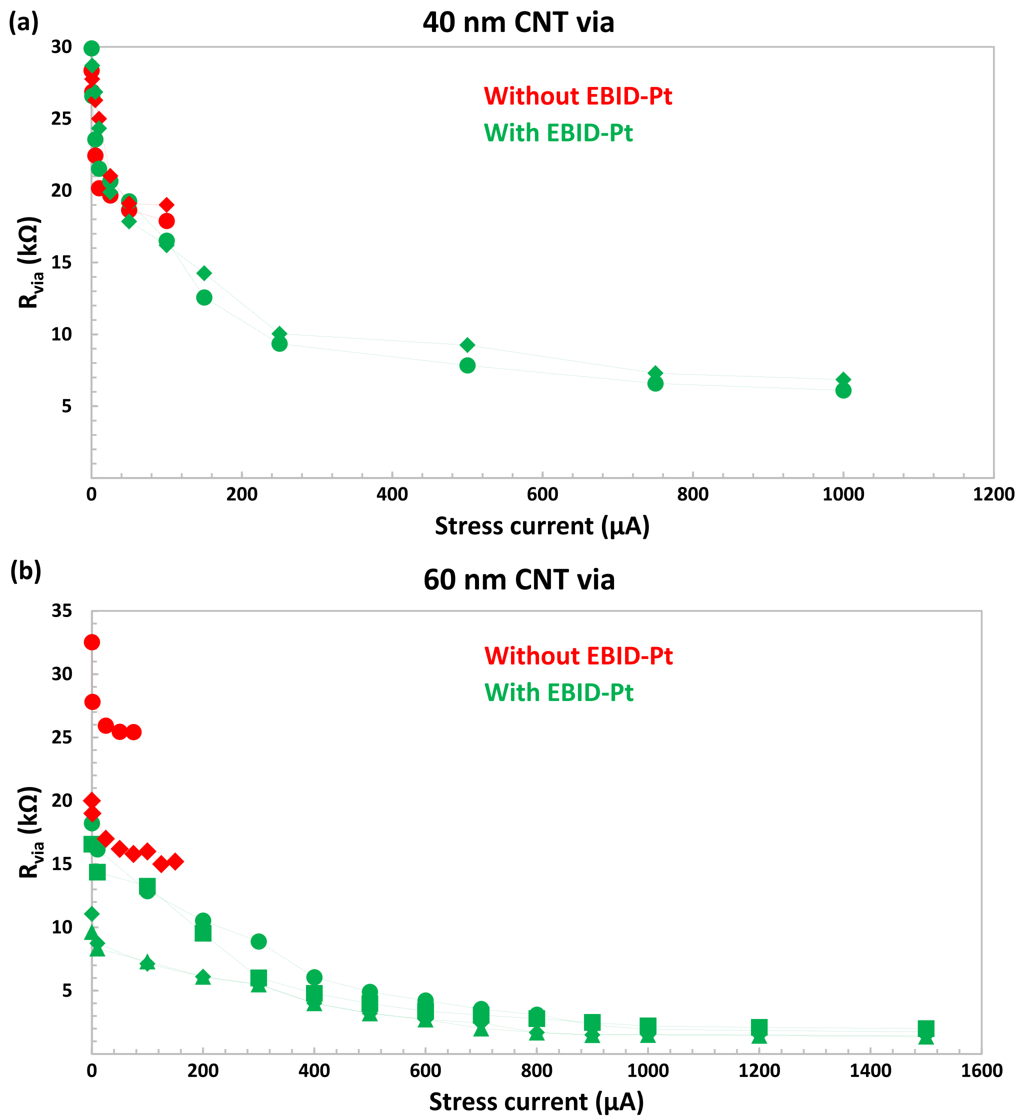

Figure 3 (a) Resistance versus stress current behavior for 40 nm vias with and without EBID-Pt top-contact. Metallization and current stressing improve and stabilize the top via contact by making conformal interfaces between the metal and exposed CNT tips, resulting in lower via resistance and improved current-carrying capacity compared to unmetallized vias. (b) Resistance versus stress current behavior for 60 nm vias with and without EBID-Pt, showing the same trend as 40 nm vias.

resulting in higher contact resistance and increased joule heating from current stressing. Furthermore, heat dissipation from the CNTs under current stressing is less efficient without the top-contact metal, and hence the via breaks down at a lower current density. An additional benefit of having a metallized via is further improvement of the top-contact by joule heat from current stressing, which facilitates the fusion of nanocrystalline grains in the metal, as observed by Wilhite [51] for EBID-W contacts and reported by Wang [56] for EBID-Pt nanocrystals. Thus, current stressing allows for local annealing of the individual vias on the test structure instead of having to thermally anneal the entire sample. Study of the horizontal CNT interconnects using end-bonded contacts after CNT growth was reported by Chiodarelli [57], showing similar improvement as in the case of horizontal carbon nanofibers after contact metallization [54]. Figure 3(a) shows the resistance behavior versus stress current for a 40 nm via, with breakdown at 1 mA. Using the average $A_{CNT} \sim 300\ nm^2$ obtained for 40 nm vias, $J_{CNT} \sim 330\ MA\ cm^{-2}$. For the 60 nm via data in figure 3(b), with an average $A_{CNT} \sim 700\ nm^2$, $J_{CNT} \sim 170\ MA\ cm^{-2}$. These via current-carrying capacities are more than two orders of magnitude higher than the J_{max} for Cu and W and are consistent with the reported values [11–13]. Table 2 summarizes the results obtained for 40 nm and 60 nm vias with and without top-contact metallization. The improvements in both via resistance and current-carrying capacity are evident for each linewidth.

The breakdown in CNTs tends to occur at defect sites [58] and can be exacerbated by ambient oxygen adsorption [59]. Therefore, the improvement of long-range order in CNTs by reducing defects and using non-oxide-based dielectric fillers can result in further enhancement in J_{CNT} as well as a reduction in via resistance. Nonetheless, the J_{CNT} values obtained in this experiment and reported by others are

Table 2. Resistance and current-carrying capacity of 40 and 60 nm vias with and without Pt top-contacts. EBID metallization stabilizes the top-contact and results in lower resistance and higher current-carrying capacity.

Via dimensions, width (nm) × height (nm)	Contact metal	Resistance (kΩ)	Current-carrying capacity (MA cm^{-2})	CNT areal density (# cm^{-2})
40 × 80	none	18	14	~10^{12}
40 × 80	none	19	14	
40 × 80	EBID Pt	6.1	330	
40 × 80	EBID Pt	6.8	330	
60 × 130	none	25	10	~3×10^{11}
60 × 130	none	15	17	
60 × 130	EBID Pt	1.4	170	
60 × 130	EBID Pt	1.7	170	
60 × 130	EBID Pt	1.4	170	
60 × 130	EBID Pt	2.0	170	

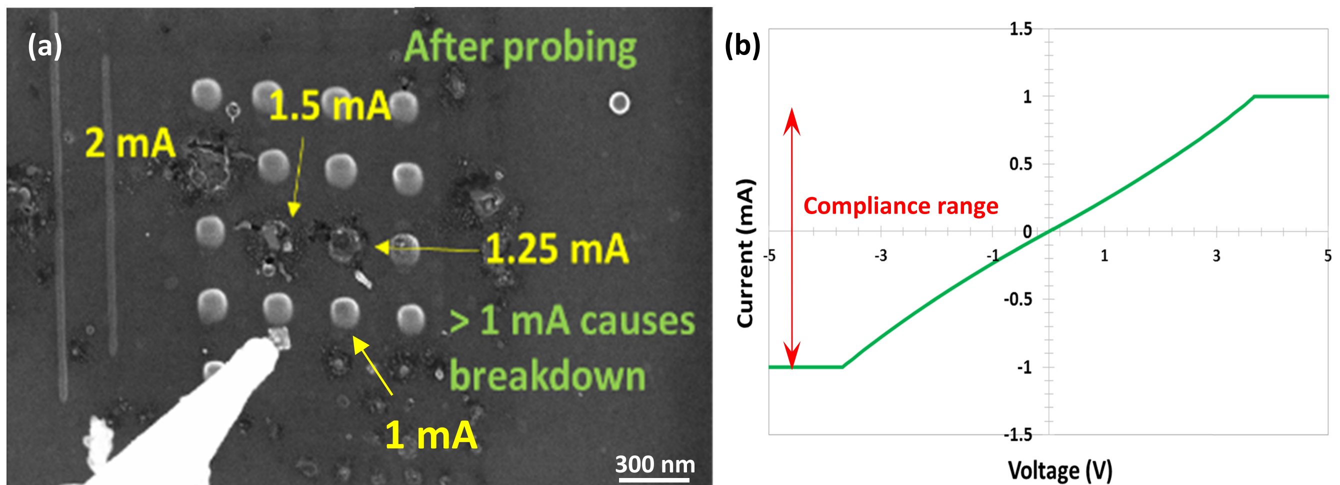

Figure 4. (a) SEM image of CNT vias after voltage sweep test. Different current ranges are used to reveal the via current capacity. Only the device with a current compliance range of ±1 mA remains intact and those with higher compliance ranges break down, confirming the measured current-carrying capacity of 330 MA cm^{-2}. (b) *I–V* sweep with current capped at ±1 mA.

more than sufficient for functionalized on-chip CNT interconnects to last through to the end of semiconductor technology nodes, if the line resistance can be reduced to approach its Cu and W counterparts. While the resistance reductions by contact metallization and similar improvements from higher CNT areal density given in table 2 are encouraging, the resistance values are still too high for integration into future technology nodes.

In order to verify the current-carrying capacity of the CNT vias obtained, a second test is conducted to determine the inherent current-carrying capacity of the CNT via without using a constant stress current. The voltage across each via is swept between a pre-defined or compliance range of currents. If a continuous linear *I–V* is obtained, it implies that the CNTs inside the via remain intact. An array of Pt-metallized vias after the voltage sweep is shown in figure 4(a). At the outset, a current compliance range of ±1 mA is used with a voltage sweep from −4 V to 4 V. As shown in figure 4(b), continuous *I–V* behavior is obtained for this compliance range. The via meeting this compliance remains intact, while those with higher compliance ranges break down as shown in figure 4(a). Thus, the current-carrying capacity shown in figure 3(a) is verified.

Finally, it is important to know how the latest results for CNT vias compare with the vias made of the conventional materials, Cu and W, with similar dimensions, and with pertinent results reported by others. A comparison of the R_{via} and J_{CNT} of CNT, Cu, and W vias with similar dimensions is given in table 3. It is clear how the CNT areal density correlates with the current-carrying capacity. However, in order to achieve higher areal density, smaller CNT diameters are needed to pack more of them into a via, which could increase the overall via resistance. Also, defects in CNTs can limit the via current-carrying capacity. It was reported that even for 700 °C growth, the defect ratio (I_D/I_G) from Raman analysis was 0.85 [52, 53]. Therefore, taller vias are susceptible to reduced current-carrying capacity as more defects are present along the CNT length, consistent with the data obtained in this work, given in table 3. Furthermore, similar to the findings on horizontal CNT interconnects [60], the dissipation of joule heat from current stressing is less efficient for a taller via, contributing to the variations in the J_{CNT} among vias with different heights. Katagiri [44, 45] reported a resistance of

Table 3. A comparison of electrical characteristics among CNT, Cu, and vias. CNT vias clearly show superior current-carrying capacities but inferior resistance—the key challenge for CNTs in replacing Cu and W in on-chip interconnects for end-of-roadmap technology nodes.

	Via dimensions (width × height)	CNT growth temperature (°C)	R_{via} (kΩ)	J_{CNT} (MA cm^{-2})	CNT areal density (# cm^{-2})	Average CNT diameter (nm)
This work	40 nm × 80 nm	700	6.1	330	10^{12}	9
	60 nm × 130 nm	700	1.7	170	3×10^{11}	20
Ref [50]	30 nm × 150 nm	700	7.8	400	1.5×10^{11}	15
Ref [44, 45]	70 nm × 100 nm	450	11	100	5×10^{11}	10
Cu [11]	30 nm × 130 nm	NA	0.025	2.5	NA	NA
W [12, 13]	30 nm × 130 nm	NA	0.060	1	NA	NA

11 kΩ and a current-carrying capacity of 100 MA cm^{-2} for a 70 nm via with CNT growth at 450 °C, while an extensive study by Vollebregt [61] conclusively demonstrated that the number of defects in CNTs increases as the growth temperature is reduced. Graham [50] reported that 700 °C CNT growth and subsequent annealing resulted in a current-carrying capacity of 400 MA cm^{-2} for a 30 nm via with a CNT areal density of 1.5×10^{11} cm^{-2}. This reported higher J_{CNT} is probably due to a multi-walled structure with a hollow interior, as evident in the cross-sectional TEM image of a CNT in [50], whereas the CNTs in our vias mostly have a 'bamboo' structure, where interlayer defects can lower their J_{max} [55, 61–63]. In all cases, while the current-carrying capacities well exceed those projected for end-of-roadmap technology nodes, via resistance and the replacement of Cu and W remain challenges, though our results suggest that further innovations in contact engineering could begin to overcome them.

4. Conclusion

CNT vias with 40 nm × 40 nm and 60 nm × 60 nm cross-sections have been fabricated and characterized to determine the via nanostructure, contact resistance, CNT resistivity, and current-carrying capacity. The contact resistance of 40 nm CNT vias has been extracted and is shown to have a similar statistical variation among vias as the total CNT area inside the via, A_{CNT}. Therefore, further contact engineering is needed to control and enhance A_{CNT} to reduce the contact resistance as well as to improve or at least maintain the via current-carrying capacity J_{CNT}. For 40 nm and 60 nm CNT vias, J_{CNT} is more than two orders of magnitude higher than Cu and W, making it a viable candidate for further development towards the functionalization of CNT interconnects. However, the via resistances reported here and by others are two orders of magnitude higher than their Cu and W counterparts. Our scheme for contact engineering suggests that further innovations in contact improvement could lead to a corresponding improvement in CNT via performance, while preserving the superiority of high current-carrying capacity to all other potential replacements for Cu and W.

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